Advanced Design System 2011.01

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1xEV Design Library

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About 1xEV Design Library

The 1xEV system, also known as HDR, is a cost effective, high-speed, high-capacity wireless technology. The system is optimized for packet data services, with a flexible architecture based on IP protocols. 1xEV can overlay an existing wireless network or work as a stand-alone system. 1xEV unleashes internet access by providing up to 2.4 Mbps in a standard bandwidth 1.25 MHz channel that is unprecedented in systems capable of fixed, portable and mobile services.

The Agilent EEsof 1xEV Design Library provides models for end-to-end system modeling and simulation of the physical layer of 1xEV systems. The models provide a baseline system for designers to get an idea of nominal ideal system performance. Also, the models can help the researchers in this field or system designers evaluate their designs and improve their work efficiency.
Features of 1xEV systems include:

- A single 1.25 MHz channel optimized for packet data results in greatest spectral efficiency
- Peak data rate of 2.4 Mbps on forward link and 307 kbps on reverse link provides unprecedented speed
- Average throughput on a loaded sector is an estimated 600 kbps on the forward link and 220 kbps on the reverse link
- Dynamically assigned data rate adjusts as fast as every 1.67 msec, providing every subscriber with the best possible rate at any given moment
- Flexible, IP-based architecture enables multiple implementation methods
- Compatible with existing CDMA networks

Agilent Instrument Compatibility

This 1xEV design library is compatible with Agilent E443xB ESG-D Series Digital RF Signal Generator and Agilent E4438C ESG Vector Signal Generator.

This 1xEV design library is also compatible with Agilent E4406A VSA Series Transmitter Tester and Agilent PSA Series High-Performance Spectrum Analyzer.

The following table shows more information of instrument models, Firmware revisions, and options.

1xEV Design Library	ESG Models	VSA Models
SpecVersion=12-2000	E443xB, Firmware Revision B.03.75	E4406A, Firmware Revision A.05.28

For more information about Agilent ESG Series of Digital and Analog RF Signal Generator and Options, please visit
http://www.agilent.com/find/ESG

For more information about Agilent E4406A VSA Series Transmitter Tester and Options, please visit
http://www.agilent.com/find/VSA

For more information about Agilent PSA Series Spectrum Analyzer and Options, please visit
http://www.agilent.com/find/PSA

Physical Layer

The reverse HDR channel, illustrated in the following figure, consists of the access channel and the reverse traffic channel.

The access channel consists of a pilot channel and a data channel. The access channel is used by the access terminal to initiate communication with the access network or to respond to an access terminal directed message.

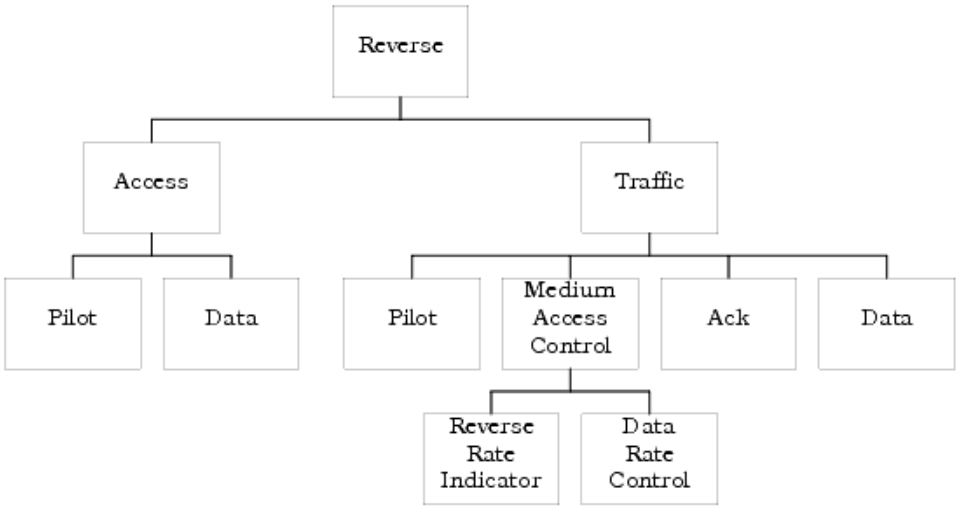
The reverse traffic channel consists of a pilot channel, a reverse rate indicator (RRI) channel, a data rate control (DRC) channel, an acknowledgement (ACK) channel, and a data channel. The reverse traffic channel is used by the access terminal to transmit user-specific traffic or signal information to the access network.

The RRI channel is used to indicate the data channel is being transmitted on the reverse traffic channel and its data rate.

The DRC channel is used by the access terminal to indicate to the access network the supportable forward traffic channel data rate and the best serving sector on the forward HDR channel.

The ACK channel is used by the access terminal to inform the access network if the data packet transmitted on the forward traffic channel has been received successfully.

Reverse Channel Structure



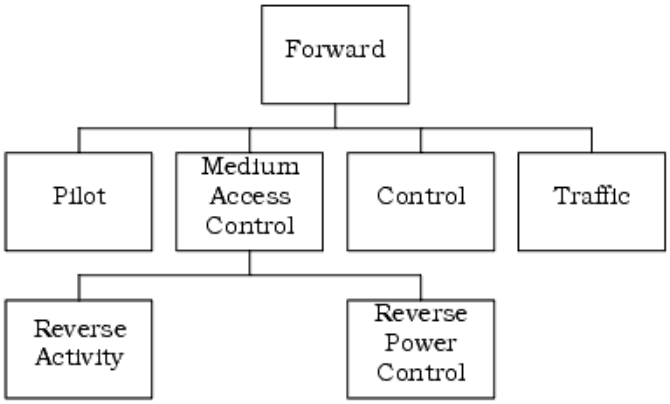
The forward HDR channel, illustrated in the following figure, consists of time-multiplexed channels: the pilot channel, the forward medium access control (MAC) channel, and the forward traffic channel or the control channel.

The traffic channel carries user data packets. The control channel carries control messages; it may also carry user traffic. Each channel is further decomposed into code-division-multiplexed quadrature Walsh channels.

The forward link consists of slots of length 2048 chips (1.66... ms). Groups of 16 slots are aligned to the PN rolls of the zero-offset PN sequences and align to system time on even-second ticks. Within each slot, the pilot, MAC, and traffic or control channels are time-division multiplexed. All time-division-multiplexed channels are transmitted at the maximum power of the sector.

The forward traffic channel is a packet-based, variable-rate channel. User data for an access terminal is transmitted at a data rate of 38.4 kbps to 2.4576 Mbps. The control channel uses 76.8 kbps and 38.4 kbps data rates.

Forward Channel Structure



Component Library Overview

The 1xEV Design Library consists of behavioral models and subnetworks organized in libraries that are described in the following sections.

Channel Coding Components

Channel coding components include CRC encoder and decoder, interleaver and Turbo encoder and decoder.

Modems

Modems library components provide modulation, Walsh and PN code generation, scrambling and spreading, rate match and signal shaping.

- 1xEV_16QAMMod and 1xEV_8PSKMod perform 16QAM and 8PSK modulation, respectively.
- 1xEV_QPSK performs quadrature spreading for forward link. Data of I and Q channels are complex multiplied against a pair of I and Q channel PN codes.
- 1xEV_HPSK performs reverse channel hybrid PSK modulation.
- 1xEV_BiWalshCode and 1xEV_WalshCode generate bi-Walsh code and Walsh code, respectively.
- 1xEV_FwdTDM and 1xEV_FwdDeTDM perform time division multiplex and de-multiplex for forward link.
- 1xEV_LgPNCode and 1xEV_PNCode generate long and short PN code, respectively. 1xEV_ScrambleCode generates a scramble sequence.
- 1xEV_BaseFilter is pulse-shaping filter on the transmit end or matched filters on the receiving end.
- 1xEV_Modulator generates QPSK, 8PSK, 16QAM modulation symbols depending on data rate. 1xEV_Demodulator demodulates the signal of QPSK, 8PSK or 16QAM and provides soft values for Turbo decoder.
- 1xEV_PhaseEqualizer provides phase equalization for the transmit signal path.
- 1xEV_RateMatch and 1xEV_RateDematch perform sequence repetition and symbol puncturing for forward link.
- 1xEV_SimplexEncoder perform simplex encoding.
- 1xEV_WalshCover performs FHT to realize Walsh cover and chip level summer. 1xEV_WalshModulator performs Walsh code modulation.

Receivers

Receiver library components provide RAKE receiving for forward and reverse links.

- 1xEV_FwdChnlEstimate performs the channel estimate for forward link and a few maximum paths are selected for maximal ratio combination.
- 1xEV_FwdMRC performs maximal ratio combination for forward link.
- 1xEV_RevChnlEstimate performs the channel estimate for reverse link and a few maximum paths are selected for maximal ratio combination.
- 1xEV_CohReceiver performance de-correlation and maximal ratio combination for reverse link.

Signal Sources

Signal Sources library components provide several kinds of signal sources.

- 1xEV_FwdSrc and 1xEV_RevSrc generate forward and reverse link signals, respectively.
- 1xEV_MAC_Src generates signal for MAC channel.
- 1xEV_FwdFrameSrc generates forward link signal in the format of data frame.

Test Components

Test library components provide BER, code domain power, Rho, and power measurements.

- 1xEV_BER measures the BER and PER for forward link and reverse link according to different data rates and slot states.
- 1xEV_FwdRhoWithRef and 1xEV_RevRhoWithRef perform Rho measurement for forward and reverse link, respectively.
- 1xEV_PwrMeasure measures the average power of the input signal.
- 1xEV_FwdCDP and 1xEV_RevCDP measures the code domain power for forward and reverse link, respectively.

Example Designs

Example designs are provided with the 1xEV Design Library, in the **/examples/1xEV** directory. Workspaces and their corresponding design examples are:

1xEV_PA_Test_wrk

- DSN_1xEV_FwdCDP
- DSN_1xEV_FwdPower
- DSN_1xEV_FwdRho
- DSN_1xEV_RevRho

1xEV_SignalSource_wrk

- DSN_1xEV_FwdCCDF
- DSN_1xEV_FwdChTest
- DSN_1xEV_FwdEVM
- DSN_1xEV_FwdFreqDomainTest
- DSN_1xEV_RevChTest
- DSN_1xEV_RevEVM

1xEV_BER_wrk

- DSN_1xEV_FwdAWGN_BER
- DSN_1xEV_RevAWGN_BER

BS_TX_wrk

- BS_TxACPR
- BS_TxCDP
- BS_TxPower
- BS_TxPowerUpgrade
- BS_TxRho
- BS_TxSpectrum

MS_RX_wrk

- MS_RxAdjacentSelectivity
- MS_RxDemodAWGN
- MS_RxDnmcRng
- MS_RxIntermodulation
- MS_RxSingleTone

MS_TX_wrk

- MS_TxACPR
- MS_TxCDP
- MS_TxPower
- MS_TxRho
- MS_TxSpectrum

Glossary of Terms

1xEV	1x system evolution
8PSK	8-ary phase shift keying
16QAM	16-ary quadrature amplitude modulation
ACPR	adjacent channel power ratio
AWGN	additive white Gaussian noise
BER	bit error rate
bps	bits per second
BS	base station
CCDF	complementary cumulative distribution function
CDMA	code division multiple access
CDP	code domain power
CRC	cyclic redundancy code
DS	direct spread
EVM	error vector magnitude
HDR	high data rate
HPSK	hybrid phase shift keying
MAC	medium access control
MS	mobile station
NRZ	non-return-to-zero
PN code	pseudo noise sequence
QPSK	quadrature phase shift keying

Base Station Transmitter Design Examples for 1xEV Design Library

Introduction

The BS_TX_wrk workspace shows 1xEV base station transmitter characteristics, including waveform quality (rho), total power, Pilot/MAC power, code domain power, conducted spurious emissions and occupied bandwidth. Designs for these include:

- BS_TxACPR for Adjacent Channel Power Ratio measurement
- BS_TxCDP for Code Domain Power measurements of MAC channel and forward traffic/control channel
- BS_TxPower for transmit power and pilot/MAC power measurements
- BS_TxPowerUpgrade with idle slot gain for transmit power and pilot/MAC power measurements
- BS_TxRho for waveform quality measurement
- BS_TxSpectrum for conducted spurious emissions and occupied bandwidth measurements

Adjacent Channel Power Ratio

BS_TxACPR

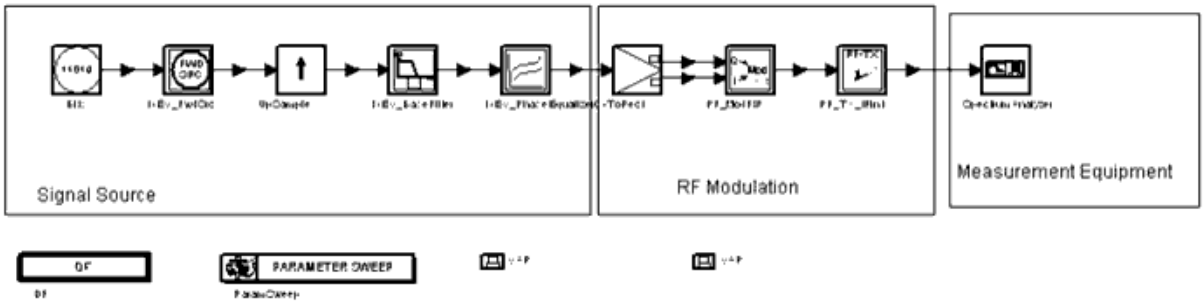
Features

- ACPR measurements for QPSK, 8PSK, and 16QAM
- ACPR measurements for idle and active slots
- Pilot, preamble, MAC channel and 4 forward traffic channels
- Signal source supports 12 data rates
- Phase equalizer

Description

This example measures ACPR for 1xEV forward link. QPSK, 8PSK, and 16QAM modulation with idle and active slot transmission modes are swept.

The schematic for this design is shown in the following figure. 1xEV_FwdSrc generates the baseband signal which is up-converted to an IF signal with RF_TX_IFin1 for measurement. The SpectrumAnalyzer component implements spectrum measurement.



BS_TxACPR Schematic

Simulation Results

Simulation results are displayed as shown in the following figure.

Eqn Res_BW_MHz=0.03

Eqn adjacent_power=spec_power(dbm(FwdSpec),(FCenter+Offset_MHz-Res_BW_MHz/2)*1e6,(FCenter+Offset_MHz+Res_BW_MHz/2)*1e6)

Eqn center_power=spec_power(dbm(FwdSpec),(FCenter-1.2288/2)*1e6,(FCenter+1.2288/2)*1e6)

Eqn ACPR_dBc= center_power-adjacent_power

FCenter
870.000 / 0.000

case	ACPR_dBc
1.000	53.394
2.000	53.394
3.000	53.394
4.000	50.679
5.000	51.443
6.000	49.708

Offset Frequence

Eqn Offset_MHz=-0.885

Note: The parameter above can be set by users according to their requirements.

Center Frequence

Eqn FCenter=FCenter_MHz[1,0]

Note: The parameter above can be set by users in corresponding design.

ACPR for 1xEV Forward Link

Benchmark

- Hardware Platform: Pentium II 333 MHz, 384 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 2002
- Simulation Time: approximately 9 minutes

References

1. 3GPP2 C.S0032, *Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network* , Initial Revision, Aug. 24, 2001.

Code Domain Power

BS_TxCDP

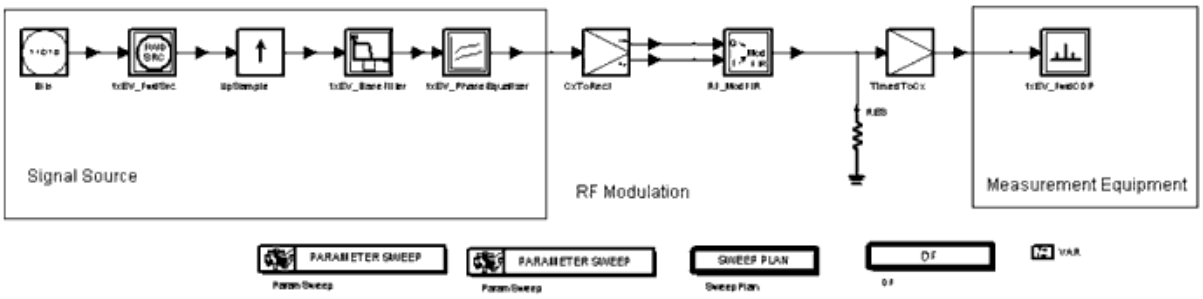
Features

- Code domain power measurements for MAC, forward traffic, and control channels
- Pilot, preamble, MAC, and 4 forward traffic channels
- Signal source supports 12 data rates
- Phase equalizer

Description

This example measures code domain power for 1xEV forward link. Code domain power is the power in each code channel of a CDMA channel. MAC, forward traffic and control channel code domain powers are swept. For forward traffic and control channel code domain power measurement, three data rates are swept: one slot version of 614.4, 1843.2, and 2457.6 kbps.

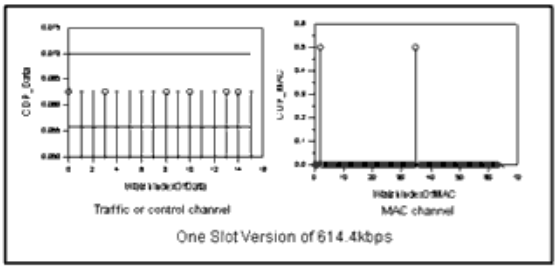
The schematic for this design is shown in the following figure. 1xEV_FwdSrc generates the baseband signal, which is up-converted to IF signal with with RF_TX_IFin for measurement. 1xEV_FwdCDP implements code domain power measurement.

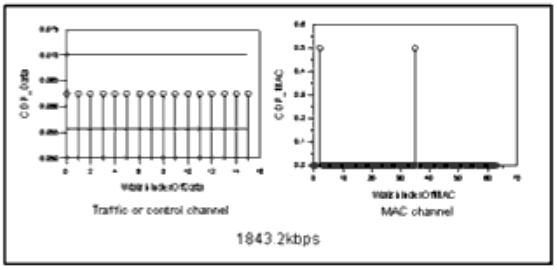


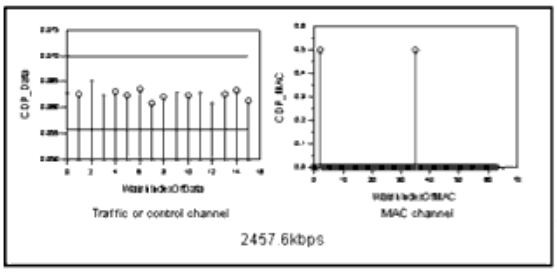
BS_TxCDP Schematic

Simulation Results

Simulation results are displayed as shown in the following figure. The *Equations* page shows the equations that are used for calculating the values of CDP. The thresholds can be set by designers according to their requirements and are displayed in the result graphs. The CDP values are compared with the thresholds and the comparison result is shown in the *Main* page as *Passed* or *Failed* .







Specification Requirement	Test Results
Please see mask definitions in page titled Equations. The test result curves should be within the masks.	Passed

Notes: Please go to page titled Equations to see the masks and the variable definitions.
Simulation time: Pentium III 800M, 512M memory, Windows NT, approximately 1.4 minutes.

Code Domain Power for 1xEV Forward Link

Benchmark

- Hardware Platform: Pentium II 333 MHz, 384 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 2002
- Simulation Time: approximately 1 minute

References

1. 3GPP2 C.S0032, *Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network* , Initial Revision, Aug. 24, 2001.

RF Output Power

BS_TxPower

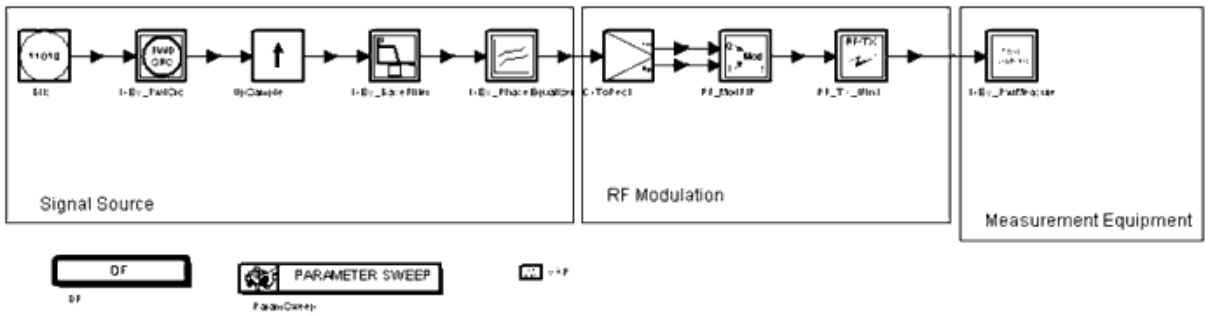
Features

- Total transmit power and pilot/MAC channel power measurement
- Pilot, preamble, MAC channel and 4 forward traffic channels
- Signal source supports 12 data rates
- Phase equalizer

Description

This example measures the total power and gated transmission characteristics for 1xEV forward link. When total power is measured, the pilot, MAC, and traffic or control channels are time-division multiplexed. All time-division multiplexed channels are transmitted at equal power. When the pilot/MAC power is measured, only pilot/MAC channels are transmitted in bursts of 224 chips every half slot.

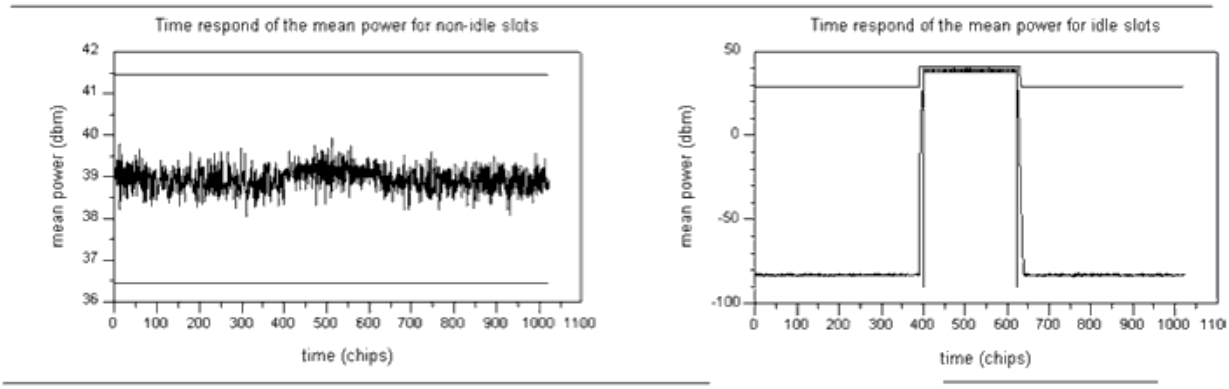
The schematic for this design is shown in the following figure. 1xEV_FwdSrc generates the baseband signal, which is up-converted to an IF signal with RF_TX_IFin1 for measurement. 1xEV_PwrMeasure implements the power measurement.



BS_TxPower Schematic

Simulation Results

Simulation results are displayed as shown in the following figure. The *Equations* page shows the equations that are used for calculating the values of transmit power. Thresholds are set according to reference [1] sections 3.1.2.3.1 and 3.1.2.3.2 and are shown in the graphs.



Transmit Power Measurement for 1xEV Forward Link

Benchmark

- Hardware Platform: Pentium II 333 MHz, 384 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 2001
- Simulation Time: approximately 5 minutes

References

1. 3GPP2 C.S0032, *Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network* , Initial Revision, Aug. 24, 2001.

RF Output Power with Idle Slot Gain

BS_TxPowerUpgrade

Features

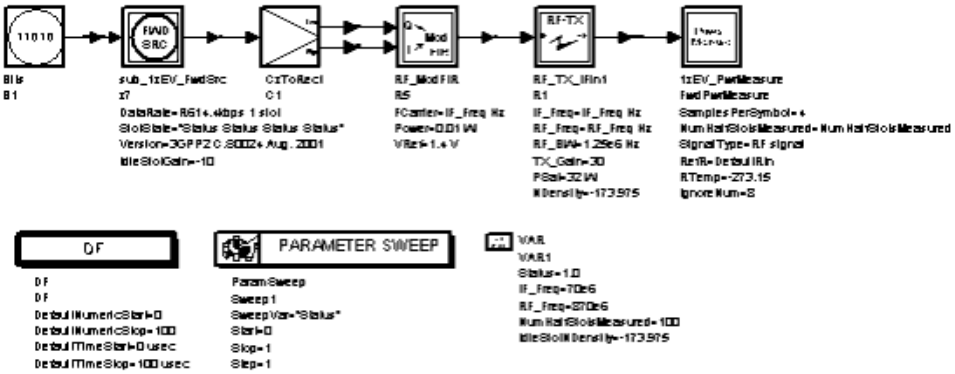
- Total transmit power and pilot/MAC channel power measurement
- Pilot, preamble, MAC channel and 4 forward traffic channels
- Signal source supports 12 data rates
- Phase equalizer
- Idle slot gain

Description

This example (same as BS_TxPower except it includes idle slot gain) measures the total power and gated transmission characteristics for 1xEV forward link. When total power is measured, the pilot, MAC, and traffic or control channels are time-division multiplexed. All time-division multiplexed channels are transmitted at equal power. When the pilot/MAC power is measured, only pilot/MAC channels are transmitted in bursts of 224 chips every half slot.
The sub_1xEV_FwdSrc generates the baseband signal, which is up-converted to an IF signal with RF_TX_IFin1 for measurement. 1xEV_PwrMeasure implements the power measurement.

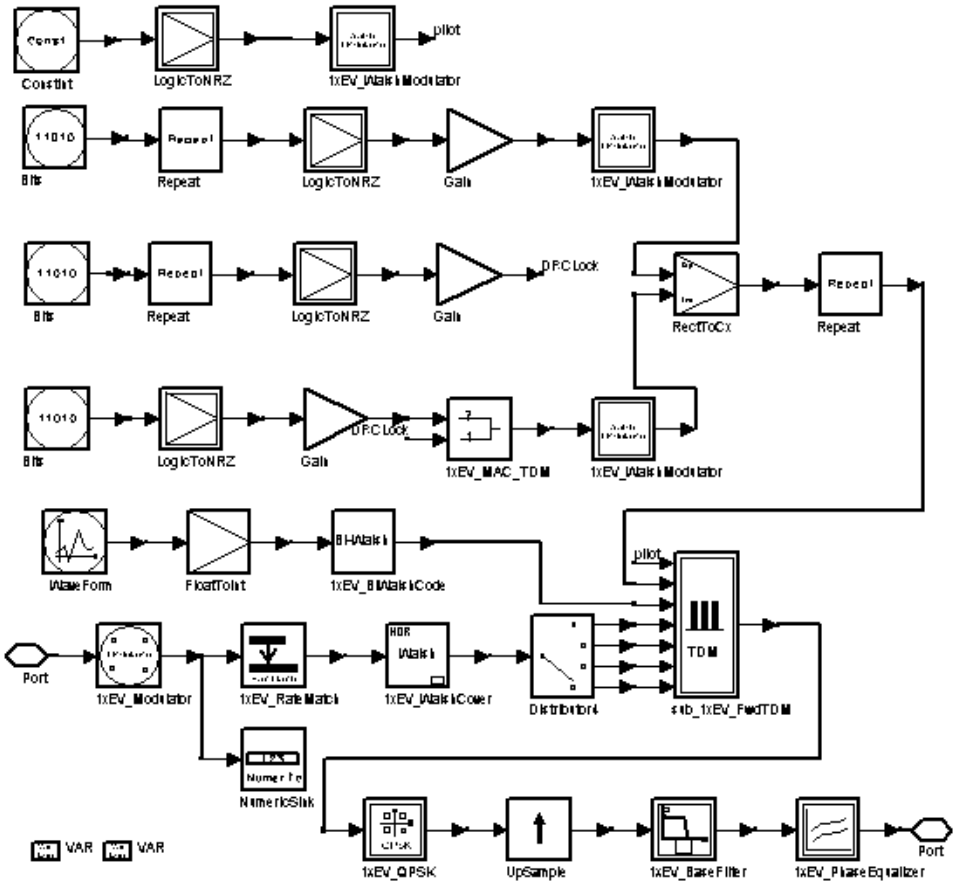
The IdleSlotGain parameter has been included in sub_1xEV_FwdSrc where specified noise power can be added to the idle slot. Idle slot gain allows the noise level during the off time of the idle slot to be varied relative to the pilot channel. By varying the idle slot gain, the on/off power ratio can be set as needed to meet the transmission envelope mask requirements of the system.

The schematic for this design is shown in the following figure.



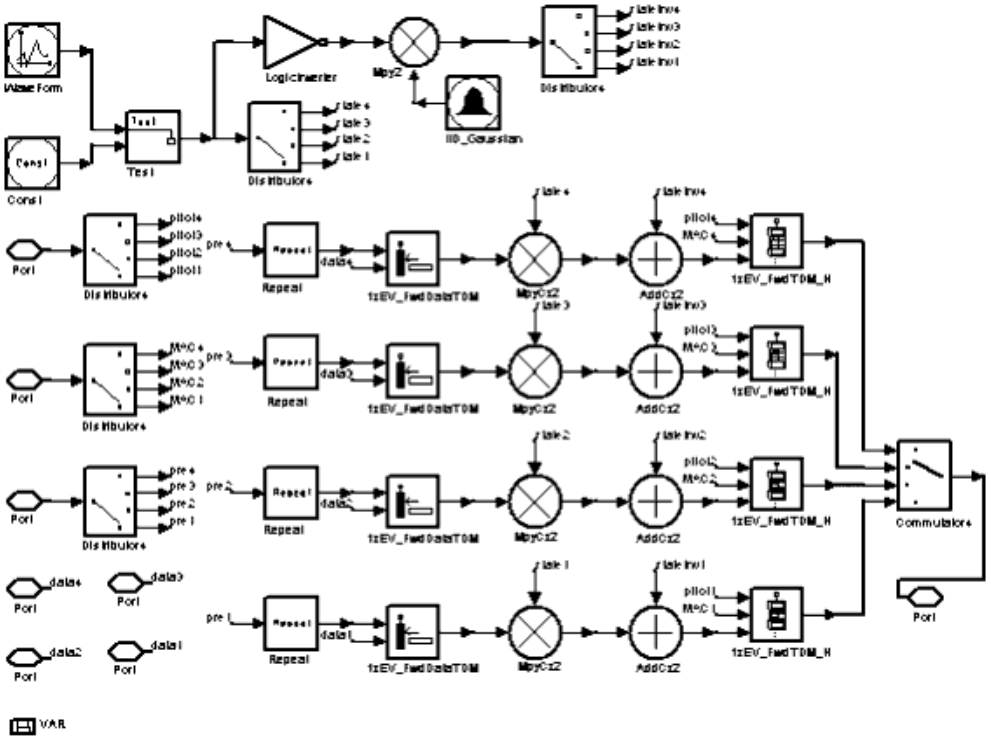
BS_TxPowerUpgrade Schematic

The sub_1xEV_FwdSrc schematic is shown in the following figure.



sub_1xEV_FwdSrc Schematic

The sub_1xEV_FwdTDM (designed for use with this workspace replaces 1xEV_FwdTDM used in BS_TXPower) is shown in the following figure. During the idle slot off period, uncorrelated noise can be added and the noise level can be varied relative to the pilot channel.

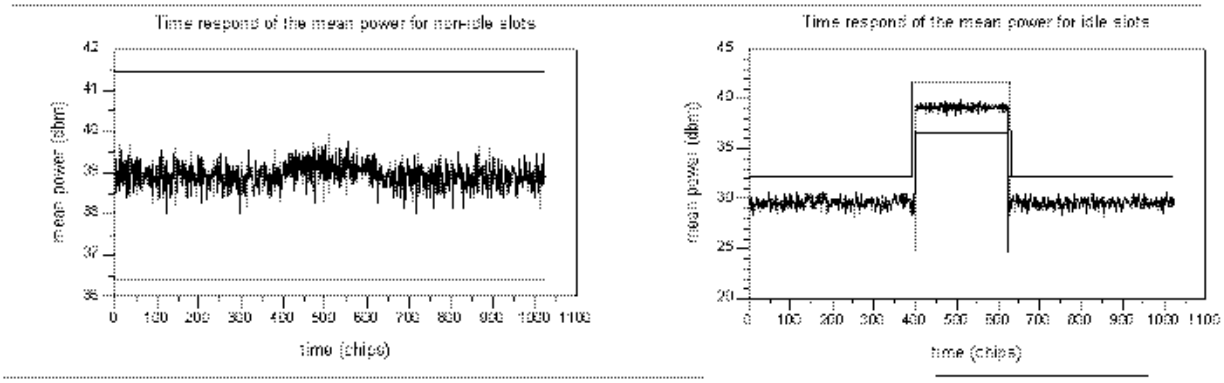


sub_1xEV_FwdTDM Schematic

Simulation Results

Simulation results are shown in the following figure.

The *Equations* page shows the equations used for calculating the values of transmit power. Thresholds, set according to reference [1] sections 3.1.2.3.1 and 3.1.2.3.2, are shown.



Transmit Power Measurement

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 2002
- Simulation Time: approximately 4 minutes

References

1. 3GPP2 C.S0032, *Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network* , Initial Revision, Aug. 24, 2001.

Waveform Quality

BS_TxRho

Features

- Normalized correlated power, Rho, measurement
- Pilot, preamble, MAC channel and 4 forward traffic channels
- Signal source supports 12 data rates
- Phase equalizer

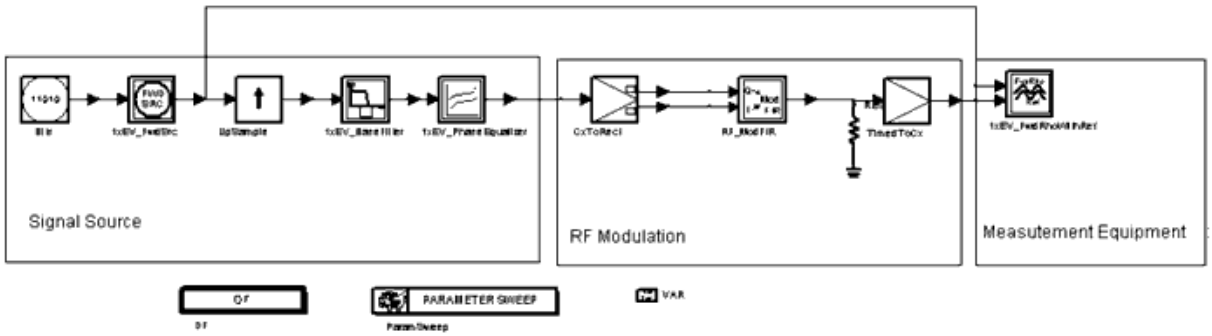
Description

This example is used to measure the waveform quality for 1xEV forward link. Waveform quality is measured by determining the normalized correlated power between the actual and the ideal waveform.

The schematic for this design is shown in the following figure. 1xEV_FwdSrc generates the baseband signal, which is up-converted to an IF signal with RF_TX_IFin1 for measurement. 1xEV_FwdRhoWithRef implements the Rho measurements.

The two data paths from the source to the measurement component are:

- one for the real transmitted signal that goes through RF modulation;
- one for the reference signal used in the measurement.



BS_TxRho Schematic

Simulation Results

Simulation results are displayed as shown in the following figure. The *Equations* page shows the equations that are used for calculating Rho. Thresholds are set according to Section 3.1.2.2.2, reference[1] and are can be set by designers according to their requirement. The comparison result is displayed in the *Main* page as *Passed* or *Failed* .

Rho_Pilot	Rho_Overall_1	Rho_Overall_2
1.000	1.000	1.000

Rho Measurement for 1xEV Forward Link

Benchmark

- Hardware Platform: Pentium II 333 MHz, 384 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 2002
- Simulation Time: approximately 1 minute

References

1. 3GPP2 C.S0032, *Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network* , Initial Revision, Aug. 24, 2001.

Transmit Spectrum and Occupied Bandwidth

BS_TxSpectrum

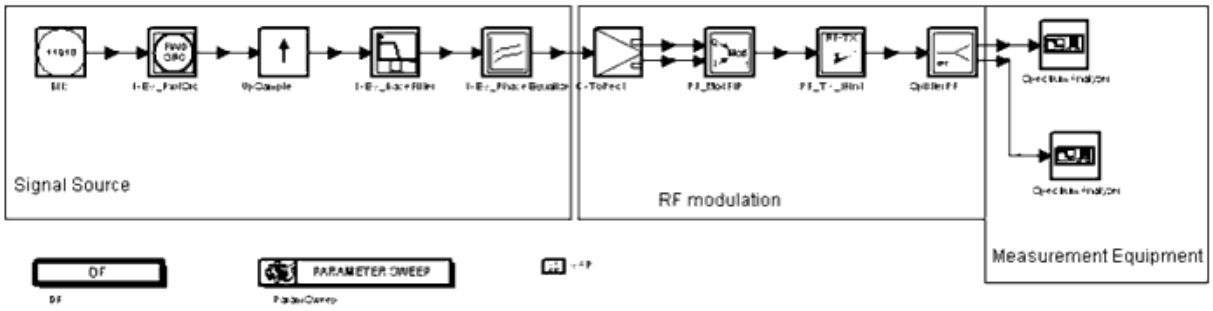
Features

- Conducted spurious emissions and occupied bandwidth measurement
- Pilot, preamble, MAC channel and 4 forward traffic channels
- Signal source supports 12 data rates
- Phase equalizer

Description

This example is used to measure conducted spurious emissions and occupied bandwidth of 1xEV forward link. Conducted spurious emissions are emissions at frequencies that are outside the assigned CDMA channel, measured at the sector RF output port. Two cases are swept: idle slots and non-idle slots. Occupied bandwidth is the frequency range, whereby the power of emissions averaged over the frequency above and under the edge frequency are 0.5% each of the total radiation power of a modulated carrier.

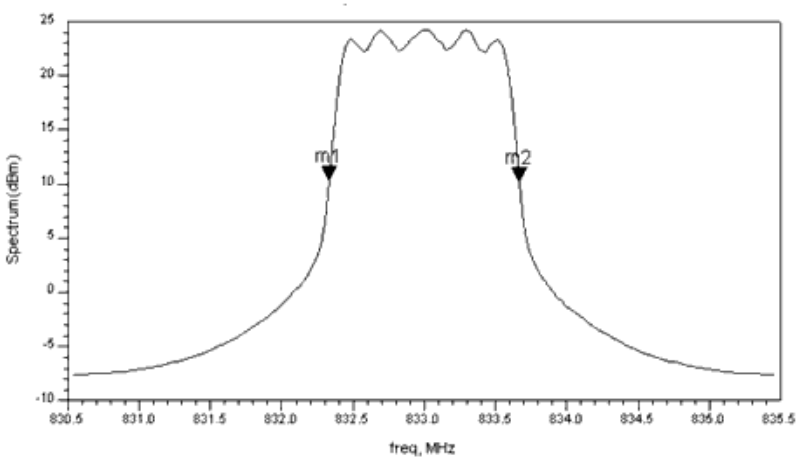
The schematic for this design is shown in the following figure. 1xEV_FwdSrc generates the base band signal, which is up-converted to an IF signal with RF_TX_IFin1 for measurement. SpectrumAnalyzer implements the spectrum measurement.



BS_TxSpectrum Schematic

Simulation Results

Simulation results are displayed in the following three figures. The *Equations* page shows the equations that are used for calculating the spectrum. The test of occupied bandwidth apply to band class 3 and 6 only; band class 3 is used in the example design and thresholds are set according to Section 3.1.2.4.1 and 3.1.2.4.4, reference[1]. If other band classes are used, the thresholds in the *Equations* page should be changed accordingly. The comparison results for conducted spurious emissions are displayed in each page as *Passed* or *Failed* .



m1
freq=832.332504MHz
dBm(FwdSpec_Band[1,::])=10.28908228

m2
freq=833.667496MHz
dBm(FwdSpec_Band[1,::])=10.22417733

Move markers with up/down arrow keys until the Lower Side and Higher Side power ratio equals to 0.5%.

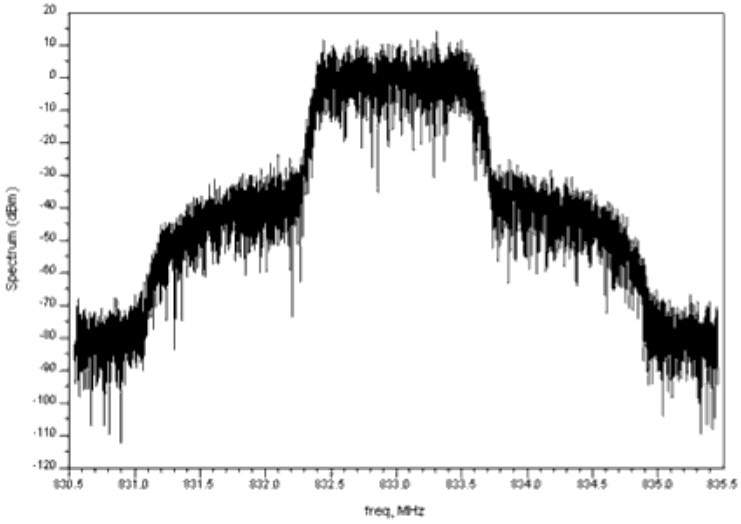
The Occupied_BW will then display the resulting bandwidth containing 99% of the transmitted power.

Lower_Side_percentage	Higher_Side_percentage	Total_Power_W
0.508405	0.502219	8.402830

Occupied_BandWidth_MHz
1.335

The occupied channel bandwidth shall be less than 1.48MHz based on a chip rate of 1.2288Mcps. The resolution bandwidth of the spectrum analyzer is 30kHz

Occupied Bandwidth for 1xEV Forward Link



Move marker with left/right arrow keys or mouse to the frequency you are interested in to find whether the transmitter emission in 30KHz at that frequency is within the limitaion specified in section 3.1.2.4.1, 3GPP2 C.S0032.

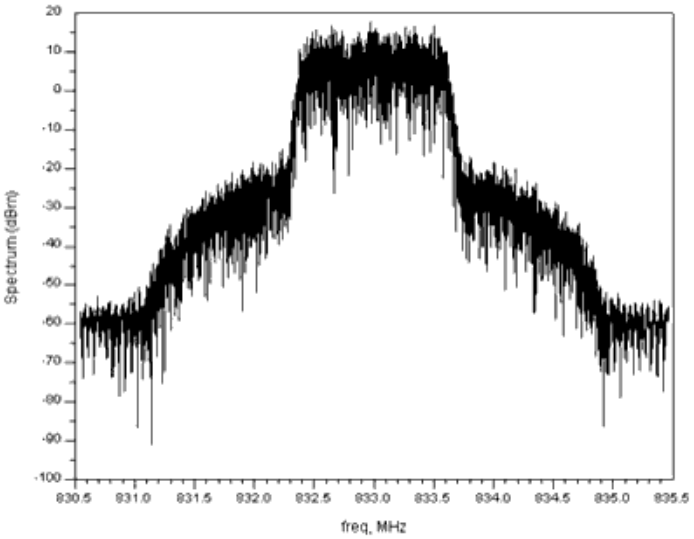
Band Class used in the example design is 3, the standard can be changed by users in the page titled 'Equations' according to their requirement for Band Class.

P30K_dBc_Idle	P30K_dBm_Idle
-59.574	-26.811

m3
freq=834.415346MHz
dBm(FwdSpec_Emission[0,::])=-44.17749553

The test result for the transmitter emission within 30KHz at this frequency is Passed

Conducted Spurious Emission for 1xEV Forward Link Idle Slots



Move marker with left/right arrow keys or mouse to the frequency you are interested in to find whether the transmitter emission in 30KHz at that frequency is within the limitaion specified in section 3.1.2.4.1, 3GPP2 C.S0032.

Band Class used in the example design is 3, the standard can be changed by users in the page titled 'Equations' according to their requirement for Band Class.

P30K_dBc_NonIdle	P30K_dBm_NonIdle
-54.999	-15.755

m4
freq=834.256307MHz
dBm(FwdSpec_Emission[1,::])=-34.30415009

The test result for the transmitter emission within 30KHz at this frequency is **Passed**

Conducted Spurious Emission for 1xEV Forward Link Non-idle Slots

Benchmark

- Hardware Platform: Pentium II 333 MHz, 384 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 2001
- Simulation Time: approximately 6 minutes

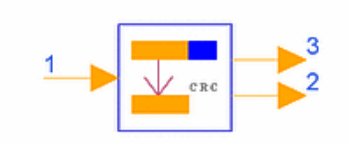
References

1. 3GPP2 C.S0032, *Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network* , Initial Revision, Aug. 24, 2001.

Channel Coding Components for 1xEV Design Library

- *1xEV CRC Decoder* (1xev)
- *1xEV CRC Encoder* (1xev)
- *1xEV FwdDeintlvr* (1xev)
- *1xEV FwdIntlvr* (1xev)
- *1xEV MAPDecoder1* (1xev)
- *1xEV MAPDecoder2* (1xev)
- *1xEV RevDeintlvr* (1xev)
- *1xEV RevIntlvr* (1xev)
- *1xEV Tail* (1xev)
- *1xEV TurboDecoder* (1xev)
- *1xEV TurboEncoder* (1xev)
- *1xEV TurboIntlvr* (1xev)
- *1xEV TurboMAPDecoder* (1xev)
- *1xEV TurboRSCEncoder* (1xev)

1xEV_CRC_Decoder



Description: CRC bits eraser with packet quality check
Library: 1xEV, Channel Coding
Class: SDF1xEV_CRC_Decoder

Parameters

Name	Description	Default	Unit	Type	Range
InputLength	input block length.	1018		int	(0, ∞)

Pin Inputs

Pin	Name	Description	Signal Type
1	Input	input data	int

Pin Outputs

Pin	Name	Description	Signal Type
2	Output	output data	int
3	PacketError	error indicator	int

Notes/Equations

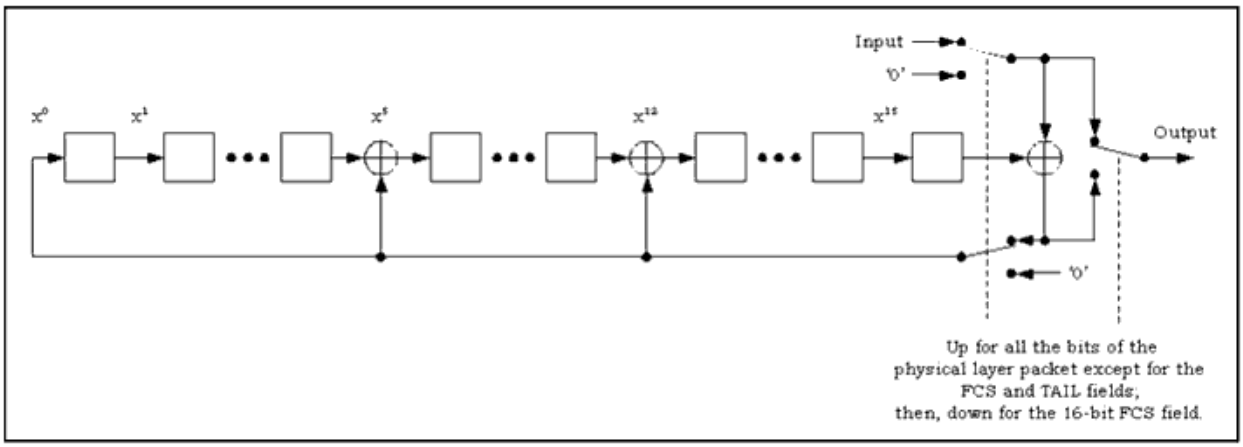
1. This model is used to erase CRC bits from the input data and check the quality of the input packet.

   Each firing, (InputLength - 16) output tokens and one PacketError token are produced for each InputLength input token consumed.
2. The FCS is used in many channels, including the control channel, the forward traffic channel, the access channel, and the reverse traffic channel. This model calculates the FCS bits of the input packet (not including received CRC bits) and compares them with the received CRC bits. If they are the same, the packet is good and PacketError output is 0; otherwise, PacketError output is 1.

   The generator polynomial for the CRC is: g(x) = x16 + x12 + x5 + 1

   The CRC are calculated according to the following procedure using the logic shown in the following figure.

   - Initially, all shift register elements are set to 0 and switches are set in the up position.
   - The register is clocked once for each bit of input data except the CRC bits. The physical layer packet is read from MSB to LSB.
   - Switches are set in the down position so that the output is a modulo-2 addition with 0; successive shift-register inputs are 0.
   - The register is clocked an additional 16 times for the 16 CRC bits.



FCS Calculation for the Physical Layer Packet

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_CRC_Encoder

Description: CRC generator
Library: 1xEV, Channel Coding
Class: SDF1xEV_CRC_Encoder

Parameters

Name	Description	Default	Unit	Type	Range
InputLength	input block length	1002		int	(0, ∞)

Pin Inputs

Pin	Name	Description	Signal Type
1	Input	input data	int

Pin Outputs

Pin	Name	Description	Signal Type
2	Output	output data	int

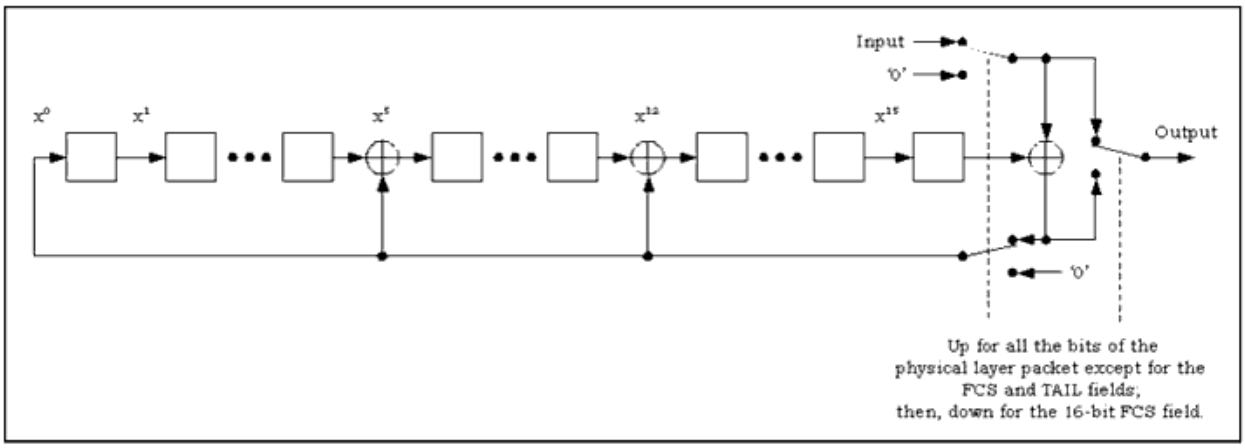
Notes/Equations

1. This model adds CRC bits after the input data and is used as the FCS generator.

   Each firing, (InputLength + 16) output tokens are produced when InputLength input tokens are consumed.
2. The FCS is used in many channels, including the control channel, the forward traffic channel, the access channel, and the reverse traffic channel. The FCS is calculated on all bits within the physical layer packet, except the FCS field itself and the encoder tail bits.

   The generator polynomial for the CRC is: g(x) = x16 + x12 + x5 + 1

   The FCS is calculated according to the following procedure using the logic shown in the following figure.
   - Initially, all shift-register elements are set to 0 and switches are set in the up position.
   - The register is clocked once for each bit of input data. The physical layer packet is read from MSB to LSB.
   - Switches are set in the down position so that the output is a modulo-2 addition with 0 and successive shift-register inputs are 0s.
   - The register is clocked an additional 16 times for the 16 FCS bits.
   - Output bits constitute all fields of the physical layer packets except the TAIL field.



FCS Calculation for the Physical Layer Packet

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_FwdDeintlvr

Description: Forward channel deinterleaver
Library: 1xEV, Channel Coding
Class: SDF1xEV_FwdDeintlvr

Parameters

Name	Description	Default	Unit	Type	Range
DataRate	forward data rate: R38.4kbps 16 slot, R76.8kbps 8 slot, R153.6kbps 4 slot, R307.2kbps 2 slot, R614.4kbps 1 slot, R307.2kbps 4 slot, R614.4kbps 2 slot, R1228.8kbps 1 slot, R921.6kbps 2 slot, R1843.2kbps 1 slot, R1228.8kbps 2 slot, R2457.6kbps 1 slot	R38.4kbps 16 slot		enum	

Pin Inputs

Pin	Name	Description	Signal Type
1	Input	the input symbol to be deinterleaved	real

Pin Outputs

Pin	Name	Description	Signal Type
2	Output	the deinterleaved symbol	real

Notes/Equations

1. This model de-interleaves forward traffic channel or control channel symbols.
2. Each firing, *N* output tokens are produced for each *N* input tokens are consumed, where *N* is the number of turbo encoder output symbols listed in the first of the two following tables.
3. This model is the inverse process of the 1xEV_FwdIntlvr. It consists of symbol permutation followed by symbol reordering. Refer to [1] for details of the process of 1xEV_FwdIntlvr.

   For code rate 1/5:
   - All input symbols are divided into three blocks denoted U, *V* 0/ *V* 0′, *V* 1/ *V* 1′. The first *N* × *CodeRate* input symbols are distributed to the *U* block, the next *N* × *CodeRate* ×2 symbols to the *V* 0/ *V* 0′ block, and the next *N* × *CodeRate* ×2 symbols to the *V* 1/ *V* 1′ block. Blocks are written in column order starting with the left-most column, top to bottom. The size of the blocks is defined in the second of the two following tables (K rows and M columns).
   - For each block the column is labeled *j* where *j* = 0, ... , *M* −1 and column 0 is the left-most column. The columns of each block are reordered so that column *j* is moved to its bit-reversed column. For example, for a 32-length array, *i* can be denoted as binary number *i* 4 *i* 3 *i* 2 *i* 1 *i* 0, with a range of 0 to 31, and *n* is a 5-bit binary number, *n* = *a* 4 *a* 3 *a* 2 *a* 1 *a* 0, where *a* 4= *i* 0, *a* 3= *i* 1, *a* 2= *i* 2, *a* 1= *i* 3, *a* 0= *i* 4. *n* is the bit reversal index of *i* .
   - The symbols of each column are end-around shifted upward by j mod k for the *U* block and by $\lfloor j/4 \rfloor$ mod k for *V* 0/ *V* 0′ and *V* 1/ *V* 1′ blocks.
   - The deinterleaver output sequence is multiplexed from the five sequences, i.e. the first output symbol is from the *U* sequence, the second from the *V* 0 sequence, the third from the *V* 1 sequence, the fourth from the *V* 0′ sequence, the fifth from the *V* 1′ sequence, the sixth from the *U* sequence, etc.

For code rate 1/3:

- All input symbols are divided into two blocks denoted *U* and *V* 0/ *V* 0′ . The first *N* × *CodeRate* input symbols are distributed to the *U* block, the next *N* × *CodeRate* ×2 symbols to the *V* 0/ *V* 0′ block. Blocks are written in column order starting with the left-most column, top to bottom. The size of the blocks are defined in in the second of the two following tables (K rows and M columns).
- For each block the column is labeled *j* , where *j* =0, ... , *M* -1 and column 0 is the left-most column. Columns of each block are reordered so that column *j* is moved to its bit-reversed column.
- The symbols of each column are end-around shifted upward by j mod k for *U* block and by $\lfloor j/4 \rfloor$ mod k for *V* 0/ *V* 0′ block.
- The deinterleaver output sequence is multiplexed by the three sequences, i.e. the first output symbol is from the *U* sequence, the second from the *V* 0 sequence, the third from the *V* 0′ sequence, the fourth from the *U* sequence, etc.

Forward Link Encoder Parameters

Data Rate (kbps)	Values per Physical Layer Packet				
	Slots	Bits	Turbo Encoder Input Bits	Code Rate	Turbo Encoder Output Symbols (N)
38.4	16	1,024	1,018	1/5	5,120
76.8	8	1,024	1,018	1/5	5,120
153.6	4	1,024	1,018	1/5	5,120
307.2	2	1,024	1,018	1/5	5,120
614.4	1	1,024	1,018	1/3	3,072
307.2	4	2,048	2,042	1/3	6,144
614.4	2	2,048	2,042	1/3	6,144
1,228.8	1	2,048	2,042	1/3	6,144
921.6	2	3,072	3,066	1/3	9,216
1,843.2	1	3,072	3,066	1/3	9,216
1,228.8	2	4,096	4,090	1/3	12,288
2,457.6	1	4,096	4,090	1/3	12,288

Channel Interleaver Parameters

Physical Layer Packet Size	U Block Interleaver Parameters		$V_0/V_{0'}$ and $V_1/V_{1'}$ Block Interleaver Parameters	
	K	M	K	M
1,024	2	512	2	1,024
2,048	2	1,024	2	2,048
3,072	3	1,024	3	2,048
4,096	4	1,024	4	2,048

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_FwdIntlvr

Description: Forward channel interleaver
Library: 1xEV, Channel Coding
Class: SDF1xEV_FwdIntlvr

Parameters

Name	Description	Default	Unit	Type	Range
DataRate	forward data rate: R38.4kbps 16 slot, R76.8kbps 8 slot, R153.6kbps 4 slot, R307.2kbps 2 slot, R614.4kbps 1 slot, R307.2kbps 4 slot, R614.4kbps 2 slot, R1228.8kbps 1 slot, R921.6kbps 2 slot, R1843.2kbps 1 slot, R1228.8kbps 2 slot, R2457.6kbps 1 slot	R38.4kbps 16 slot		enum	

Pin Inputs

Pin	Name	Description	Signal Type
1	Input	the symbol to be interleaved	int

Pin Outputs

Pin	Name	Description	Signal Type
2	Output	the interleaved symbol	int

Notes/Equations

1. This model interleaves forward traffic channel or control channel symbols. The input symbols are coded data which is scrambled.
2. Each firing, N output tokens are produced when N input tokens are consumed, where N is the number of turbo encoder output symbols listed in the table of Forward Link Encoder Parameters below.
3. This model consists of symbol reordering followed by symbol permuting.

   For code rate 1/5:
   - All the input symbols are sequentially demultiplexed into five sequences denoted U, V_0, V_1, V_0', V_1', that is, the first input symbol is distributed to the U sequence, the second to the V_0 sequence, the third to the V_1 sequence, the fourth to the V_0' sequence, the fifth to the V_1' sequence, the sixth to the U sequence, etc.
   - U, V_0, V_1, V_0', V_1' sequences are ordered according to U, V_0, V_0', V_1, V_1'.
   - Reordered symbols are permuted in three separate blocks $U, V_0/V_0', V_1/V_1'$. The size of the blocks is defined in the table of Channel Interleaver Parameters below (K rows and M columns). The entire sequence of symbols is written to the three blocks respectively by rows starting from the top row, and from left to right.
   - For each block the column is labeled j where $j = 0, \ldots, M-1$ and column 0 is the left-most column. Symbols of each column are then end-around shifted downward by j mod k for the

U block and by $\lfloor j/4 \rfloor$ mod k for V_0/V_0' and V_1/V_1' blocks.

- Results are read out by column with addresses based on column bit reversal index 0 to $M-1$ and top to bottom. The interleaver output sequence is the interleaved U symbols, followed by the interleaved V_0/V_0' symbols, followed by the interleaved V_1/V_1' symbols.

For code rate 1/3:

- All input symbols are sequentially demultiplexed into three sequences U, V_0, V_0', that is, the first input symbol is distributed to the U sequence, the second to the V_0 sequence, the third to the V_0' sequence, the fourth to the U sequence, and so on.
- Symbols are permuted in two separate blocks $U, V_0/V_0'$. The size of the blocks is defined in the table of Channel Interleaver Parameters below (K rows and M columns). The entire sequence of symbols is written to the two blocks respectively by rows starting from the top row, and from left to right.
- For each block the column is labeled j where $j = 0, \ldots, M-1$ and column 0 is the left-most column. Symbols of each column are then end-around shifted downward by j mod k for the U block and by $\lfloor j/4 \rfloor$ mod k for V_0/V_0' block.
- Results are read out by column with addresses based on column bit reversal index 0 to $M-1$ and top to bottom. The interleaver output sequence is the interleaved U symbols followed by the interleaved V_0/V_0' symbols.

Forward Link Encoder Parameters

Data Rate (kbps)	Values per Physical Layer Packet				
	Slots	Bits	Turbo Encoder Input Bits	Code Rate	Turbo Encoder Output Symbols (N)
38.4	16	1,024	1,018	1/5	5,120
76.8	8	1,024	1,018	1/5	5,120
153.6	4	1,024	1,018	1/5	5,120
307.2	2	1,024	1,018	1/5	5,120
614.4	1	1,024	1,018	1/3	3,072
307.2	4	2,048	2,042	1/3	6,144
614.4	2	2,048	2,042	1/3	6,144
1,228.8	1	2,048	2,042	1/3	6,144
921.6	2	3,072	3,066	1/3	9,216
1,843.2	1	3,072	3,066	1/3	9,216
1,228.8	2	4,096	4,090	1/3	12,288
2,457.6	1	4,096	4,090	1/3	12,288

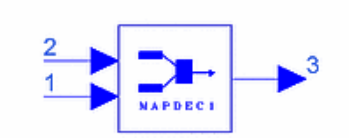
Channel Interleaver Parameters

Physical Layer Packet Size	U BlockInterleaver Parameters		$V_0/V_{0'}$ and $V_1/V_{1'}$ Block Interleaver Parameters	
	K	M	K	M
1,024	2	512	2	1,024
2,048	2	1,024	2	2,048
3,072	3	1,024	3	2,048
4,096	4	1,024	4	2,048

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_MAPDecoder1



Description: MAP decoder 1 for turbo decoder
Library: 1xEV, Channel Coding
Class: SDF1xEV_MAPDecoder1

Parameters

Name	Description	Default	Symbol	Unit	Type	Range
BlockSize	turbo block size	250	L		int	[1:65536]
ConstraintLength	constraint length of RSC encoder in turbo encoder	4	K		int	[3:9]
Polynomial	generator polynomial	015 013 017			int array	

Pin Inputs

Pin	Name	Description	Signal Type
1	D_In	input data	real
2	PriIn	input priori information	real

Pin Outputs

Pin	Name	Description	Signal Type
3	Post	output log-likelihood ratio LLR	real

Notes/Equations

1. This model performs turbo code decoding with MAP algorithm (Maximum A Posterior). It is a modified BCJR algorithm for RSC code. Two parallel concatenated MAP decoders constitute the turbo code decoder. If the Polynomial parameter has M components, then the code rate of the component code of turbo code will be 1/M.

   Each firing, L Post tokens are produced when L×M D_In tokens and L PriIn tokens are consumed.
2. The Polynomial parameter specifies the generator polynomial of the recursive system encoder, as described in the following.

   Assuming a RSC encoder has transfer function

   $$G(D) = [1, \frac{n_0(D)}{d(D)}, \frac{n_1(D)}{d(D)}]$$

   where d(D) = 1 + D^2 + D^3 , n_0 (D) = 1 + D + D^3, and n_1 (D) = 1 + D + D^2 + D^3. The binary value of d(D), n_0 (D) and n_1 (D) are the first, second and third components of the Polynomial vector, respectively.

   Writing out the coefficient sequence of an equation from the highest to the lowest order, one obtains the binary form of the equation, with the most significant bit (MSB) corresponding to the coefficient of the highest order item. For example:

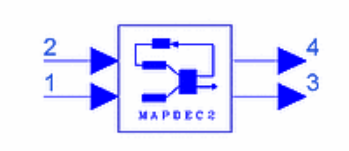
- the value for d(D) is 1101(B) = 015(O) = 0x0D(H)= 13(D)
- the value for n_0 (D) is 1011(B) = 013(O) = 0x0B(H) = 11(D)
- the value for n_1 (D) is 1111(B) = 017(O) = 0x0F(H) = 15(D).

Thus, the Polynomial setting is 015 013 017, 0x0D,0x0B,0x0F or 13,11,15.

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.
2. L.R. Bahl, J. Cocke, F. Jeinek and J. Raviv. "Optimal decoding of linear codes for minimizing symbol error rate," *IEEE Trans. Inform. Theory* , vol. IT-20. pp.248-287, March 1974.
3. C. Berrou, A. Glavieux, and P. Thitimjshima, "Near Shannon limit error correcting coding: Turbo codes," *IEEE International Conference on Communications* , pp. 1064-1070, May 1993.

1xEV_MAPDecoder2



Description: MAP decoder 2 for turbo decoder
Library: 1xEV, Channel Coding
Class: SDF1xEV_MAPDecoder2

Parameters

Name	Description	Default	Symbol	Unit	Type	Range
BlockSize	turbo block size	250	L		int	[1:65536]
ConstraintLength	constraint length of RSC encoder in turbo encoder	4	K		int	[3:9]
Polynomial	generator polynomial	015 013 017			int array	

Pin Inputs

Pin	Name	Description	Signal Type
1	D_In	input parity signal	real
2	PriIn	input priori information	real

Pin Outputs

Pin	Name	Description	Signal Type
3	Post	output log-likelihood ratio LLR	real
4	PriOut	output priori information to Decoder1	real

Notes/Equations

1. This model performs turbo code decoding with MAP algorithm (Maximum A Posterior). It is a modified BAHL et al. algorithm for RSC codes. Two parallel concatenated MAP decoders constitute the turbo code decoder. If the Polynomial parameter has M components, then the code rate of the component code of turbo code will be 1/M.

   Each firing, L Post tokens and L PriOut tokens are produced when L×(M-1) D_In tokens and L PriIn tokens are consumed.
2. The Polynomial parameter specifies the generator polynomial of the recursive system encoder, as described in the following.

   Assuming a RSC encoder has transfer function

   $$G(D) = [1, \frac{n_0(D)}{d(D)}, \frac{n_1(D)}{d(D)}]$$

   where $d(D) = 1 + D^2 + D^3$, $n_0(D) = 1 + D + D^3$, and $n_1(D) = 1 + D + D^2 + D^3$. The binary value of d(D), $n_0(D)$ and $n_1(D)$ are the first, second and third components of the Polynomial vector, respectively.

   Writing out the coefficient sequence of an equation from the highest to the lowest order, one

obtains the binary form of the equation, with the most significant bit corresponding to the coefficient of the highest order item. For example:

- the value for d(D) is 1101(B) = 015(O) = 0x0D(H) = 13(D)
- the value for n_0(D) is 1011(B) = 013(O) = 0x0B(H) = 11(D)
- the value for n_1(D) is 1111(B) = 017(O) = 0x0F(H) = 15(D)

Thus the Polynomial setting is 015 013 017, 0x0D,0x0B,0x0F or 13,11,15.

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.
2. L.R. Bahl, J. Cocke, F. Jeinek, and J. Raviv. "Optimal decoding of linear codes for minimizing symbol error rate," *IEEE Trans. Inform. Theory* , vol. IT-20. pp.248-287, March 1974.
3. C.Berrou, A.Glavieux, and P. Thitimjshima, "Near Shannon limit error correcting coding: Turbo codes," *IEEE International Conference on Communications* , pp. 1064-1070, May 1993.

1xEV_RevDeintlvr

Description: Reverse channel deinterleaver
Library: 1xEV, Channel Coding
Class: SDF1xEV_RevDeintlvr

Parameters

Name	Description	Default	Unit	Type	Range
InputLength	the input data length	1024		int	(0, ∞)

Pin Inputs

Pin	Name	Description	Signal Type
1	Input	the input symbol to be deinterleaved	real

Pin Outputs

Pin	Name	Description	Signal Type
2	Output	the deinterleaved symbol	real

Notes/Equations

1. This model de-interleaves reverse data channel symbols.
2. Each firing, InputLength tokens are produced when InputLength tokens are consumed. InputLength must be a power of 2.
3. This model is the inverse process of 1xEV_RevIntlvr.

   A linear sequential array of InputLength is formed and written with addresses from 0 to InputLength - 1. The array is read with addresses based on bit-reversal index.

   Bit-reversal rearranges the input array, of which length is a power of 2. The index (decimal) is converted into binary numbers. For a 32-length array, i can be denoted as binary number $i_4 i_3 i_2 i_1 i_0$, with a range of 0 to 31, and n is a 5-bit binary number, $n = a_4 a_3 a_2 a_1 a_0$, where $a_4 = i_0$, $a_3 = i_1$, $a_2 = i_2$, $a_1 = i_3$, $a_0 = i_4$. n is the bit reversal index of i. This function rearranges the input array by exchanging the number of index i for the number of bit reversal index n.

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_RevIntlvr

Description: Reverse channel interleaver
Library: 1xEV, Channel Coding
Class: SDF1xEV_RevIntlvr

Parameters

Name	Description	Default	Unit	Type	Range
InputLength	the input data length	1024		int	(0, ∞)

Pin Inputs

Pin	Name	Description	Signal Type
1	Input	the symbol to be interleaved	int

Pin Outputs

Pin	Name	Description	Signal Type
2	Output	the interleaved symbol	int

Notes/Equations

1. This model interleaves reverse data channel symbols. The input data is the output sequence from the encoder.
2. Each firing, InputLength tokens are produced when InputLength tokens are consumed. InputLength must be a power of 2.
3. This interleaver uses bit-reversal.

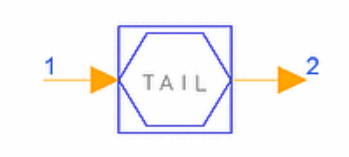
   A linear sequential array with of InputLength is formed and written with addresses from 0 to InputLength - 1. The array is read with addresses based on bit reversal index.

   Bit-reversal rearranges the input array, of which length is a power of 2. The index (decimal) is converted into binary numbers. For a 32-length array, i can be denoted as binary number $i_4 i_3 i_2 i_1 i_0$, with a range of 0 to 31, and n is a 5-bit binary number, $n = a_4 a_3 a_2 a_1 a_0$, where $a_4 = i_0$, $a_3 = i_1$, $a_2 = i_2$, $a_1 = i_3$, $a_0 = i_4$. n is the bit reversal index of i. This function rearranges the input array by exchanging the number of index i for the number of bit reversal index n.

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_Tail



Description: Tailing bits adder or remover
Library: 1xEV, Channel Coding
Class: SDF1xEV_Tail

Parameters

Name	Description	Default	Unit	Type	Range
AddRmvSwitch	switch between adding and removing tail bits: Add, Remove	Add		enum	
InputLength	input data length	1018		int	(0, ∞)
TailLength	tail bits length	6		int	†

† TailLength should be in the range of [0, + inf) when AddRmvSwitch=Add, and in the range of [0, InputLength-1] when AddRmvSwitch=Remove.

Pin Inputs

Pin	Name	Description	Signal Type
1	Input	input data	int

Pin Outputs

Pin	Name	Description	Signal Type
2	Output	output data	int

Notes/Equations

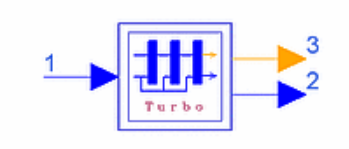
1. This model adds or removes tail bits.
2. If AddRmvSwitch=Add, (InputLength + TailLength) output tokens are produced when InputLength tokens are consumed; if AddRmvSwitch=Remove, (InputLength-TailLength) tokens are produced when InputLength tokens are consumed.

   If AddRmvSwitch = Add, TailLength tokens are added after every InputLength input tokens, and the tail bits are all 0; if AddRmvSwitch = Remove, TailLength tokens are removed from every InputLength input tokens. Therefore, TailLength must be less than InputLength.

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_TurboDecoder



Description: 4-Level turbo decoder
Library: 1xEV, Channel Coding
Class: SDF1xEV_TurboDecoder

Parameters

Name	Description	Default	Symbol	Unit	Type	Range
PacketLength	output packet length (not including 6 tail bits)	250	N		int	{250,506,1018,2042,3066,4090}
CodeRate	code rate of turbo code: CodeRate1/2, CodeRate1/3, CodeRate1/4, CodeRate1/5	CodeRate1/2			enum	

Pin Inputs

Pin	Name	Description	Signal Type
1	D_In	input data	real

Pin Outputs

Pin	Name	Description	Signal Type
2	PriOut	priori value for next decoder	real
3	BitOut	decoded bits	int

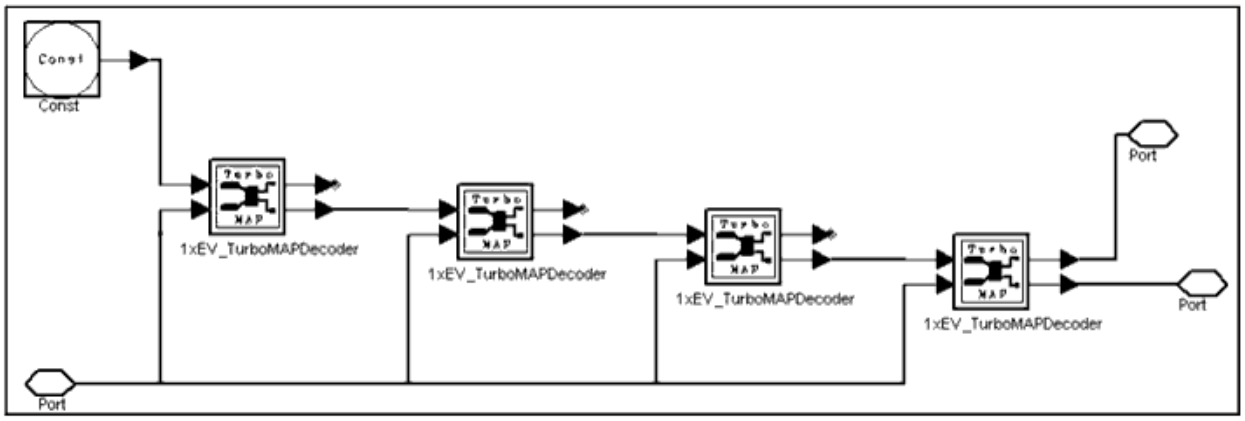
Notes/Equations

1. This subnetwork is used to implement 4-level iterative MAP decoding algorithm for turbo code. The schematic for this subnetwork is shown in the following figure. The turbo decoder is concatenated by four 1xEV_TurboMAPDecoders to construct a multi-level decoder.

   This subnetwork can be used to construct an arbitrary level decoder to meet performance demands or the designer's iterative convergence criterion.

   The signal polluted by channel noise is input at pin D_In and the decoded signal is output at pin BitOut.

   The 1xEV_TurboMAPDecoder calculate the log-likelihood ratio (LLR) according to a priori information and signal polluted by the channel noise using the BCJR algorithm [2]. Passing the sign sequence of the LLR through a NRZtoLogic model (which maps 1 to 0 and -1 to 1) and a de-interleaver obtains the decoded signal, which is output at pin BitOut from 1xEV_TurboMAPDecoder. The extrinsic information, which can be used as a priori information in the next level decoder if necessary, is output at pin PriOut of 1xEV_TurboMAPDecoder.

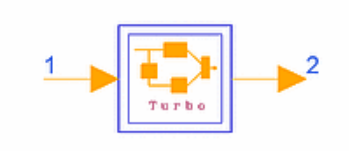


1xEV_TurboDecoder Schematic

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.
2. L.R. Bahl, J. Cocke, F. Jeinek and J. Raviv. "Optimal decoding of linear codes for minimizing symbol error rate," *IEEE Trans. Inform* . Theory, vol. IT-20. pp.248-287, Mar. 1974.
3. C.Berrou, A. Glavieux, and P. Thitimjshima, "Near Shannon limit error correcting coding: Turbo codes," *IEEE International Conference on Communications* , pp. 1064-1070, May 1993.

1xEV_TurboEncoder



Description: Turbo Encoder
Library: 1xEV, Channel Coding
Class: SDF1xEV_TurboEncoder

Parameters

Name	Description	Default	Symbol	Unit	Type	Range
PacketLength	input packet length including 6 tail bits	256	N		int	{256,512,1024,2048,3072,4096}
CodeRate	code rate of turbo code: CodeRate1/2, CodeRate1/3, CodeRate1/4, CodeRate1/5	CodeRate1/2			enum	

Pin Inputs

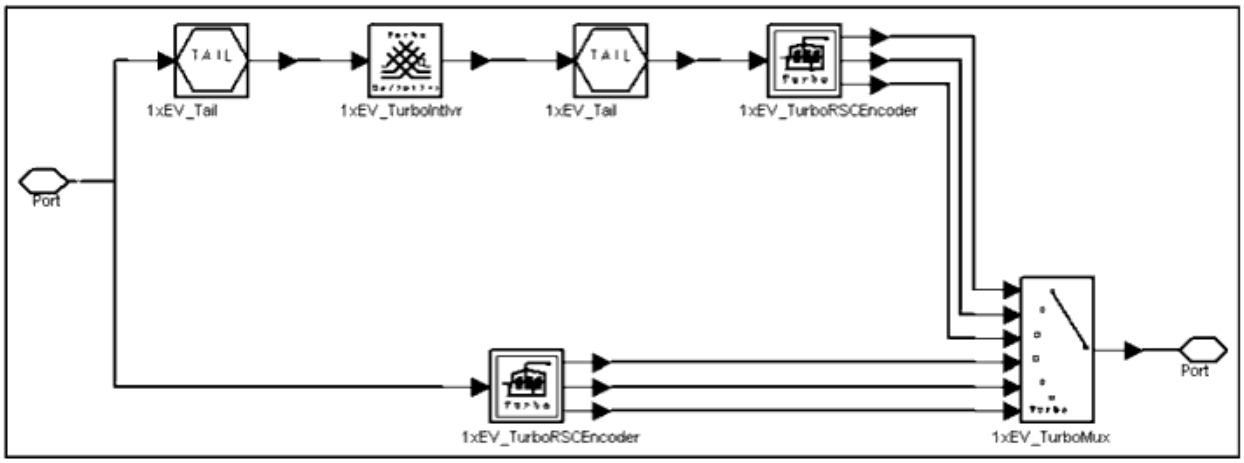
Pin	Name	Description	Signal Type
1	D_In	input data	int

Pin Outputs

Pin	Name	Description	Signal Type
2	D_Out	output data	int

Notes/Equations

1. This subnetwork is used as turbo encoder. The schematic for this subnetwork is shown in the following figure.



1xEV_TurboEncoder Schematic

2. The turbo encoder uses two parallel concatenated recursive systematic convolutional (RSC) encoders with an interleaver before the second RSC encoder. The two recursive convolutional

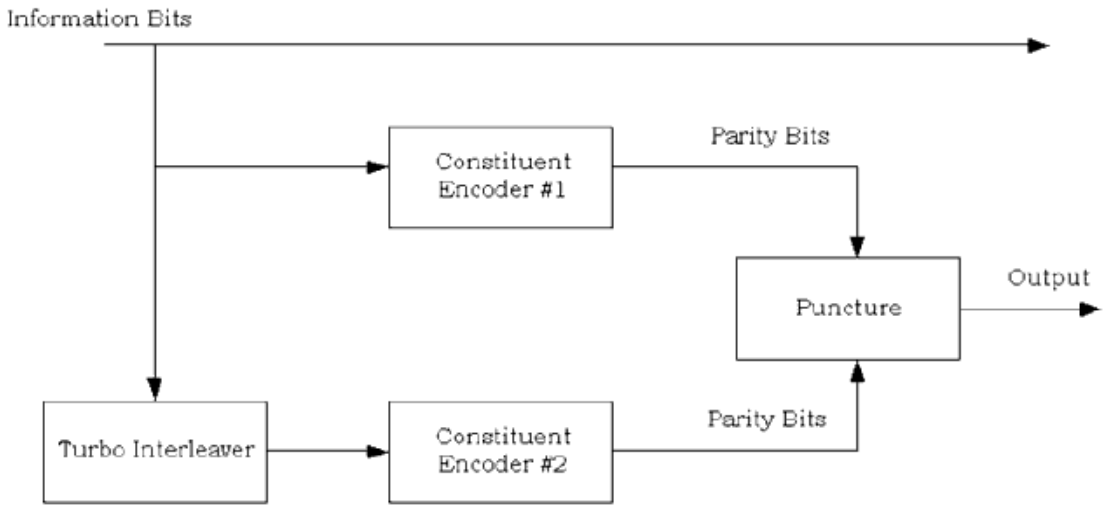
codes are named the constituent codes of the turbo code. Outputs of the constituent encoders are punctured and repeated to achieve (Nturbo + 6)/R output symbols, where Nturbo is turbo interleaver block size, with value N-6.

A common constituent code (RSC Code) is used for turbo codes of rate 1/2, 1/3, 1/4 or 1/5. The transfer function for the constituent code is

$$G(D) = [1, \frac{n_0(D)}{d(D)}, \frac{n_1(D)}{d(D)}]$$

where d(D) = 1 + D2 + D3, n0(D) = 1 + D + D3, and n1(D) = 1 + D + D2 + D3.

The turbo encoder generates an output symbol sequence that is identical to the one generated by the encoder shown in the following figure. Initially, the states of the constituent encoder registers in this figure are set to zero.

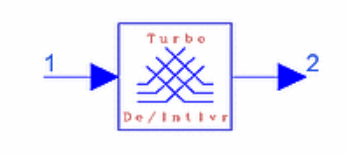


General Turbo Code Encoder

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_TurboIntlvr



Description: Interleaver or De-interleaver for turbo code
Library: 1xEV, Channel Coding
Class: SDF1xEV_TurboIntlvr

Parameters

Name	Description	Default	Symbol	Unit	Type	Range
BlockSize	turbo block size	250	Nturbo		int	[129:4096]
Type	interleave type: Interleave, De-interleave	Interleave			enum	

Pin Inputs

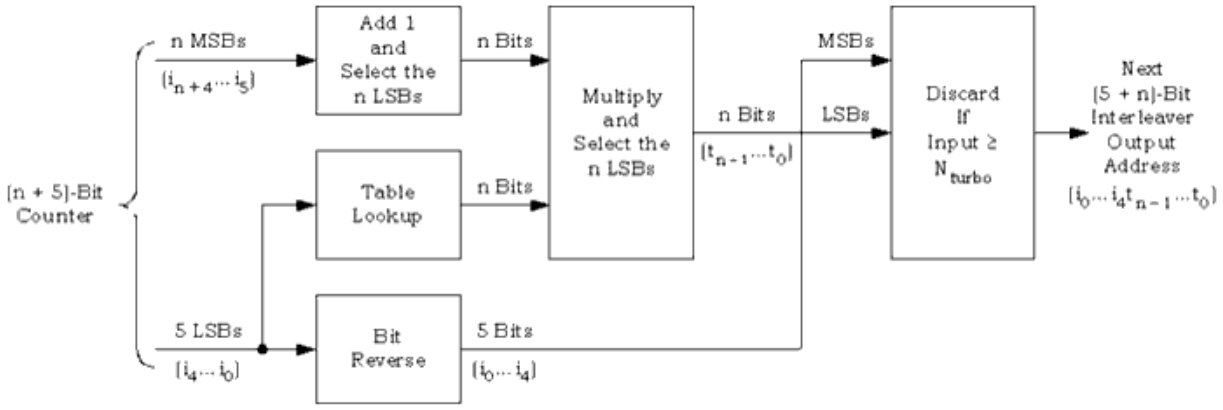
Pin	Name	Description	Signal Type
1	D_In	input sequence for interleaving or de-interleaving	real

Pin Outputs

Pin	Name	Description	Signal Type
2	D_Out	output interleaved or de-interleaved sequence	real

Notes/Equations

1. This model interleaves or de-interleaves the input sequence for turbo code. Each firing, Nturbo D_Out tokens are produced when Nturbo D_In tokens are consumed.
2. The entire sequence of turbo interleaver input bits are written sequentially into an array at a sequence of addresses; the entire sequence is then read out from a sequence of addresses. Let the sequence of input addresses be from 0 to Nturbo -1, where Nturbo is the number of symbols in the turbo interleaver. The sequence of interleaver output addresses is equivalent to those generated according to the following steps and illustrated in the following figure.



Turbo Interleaver Output Address Calculation

Step 1. Determine the turbo interleaver parameter, n, where n is the smallest integer such that Nturbo ≤ $2^{(n + 5)}$. The first of the two tables below gives this parameter.
Step 2. Initialize an (n + 5)-bit counter to 0.
Step 3. Extract the n most significant bits (MSBs) from the counter and add one to form a new value. Then, discard all except the n least significant bits (LSBs) of this value.
Step 4. Obtain the n-bit output of the table lookup defined in the second of the two tables below with a read address equal to the five LSBs of the counter. Note that this table depends on the value of n.
Step 5. Multiply the values obtained in Steps 3 and 4, and discard all except the n LSBs.
Step 6. Bit-reverse the five LSBs of the counter.
Step 7. Form a tentative output address that has its MSBs equal to the value obtained in Step 6 and its LSBs equal to the value obtained in Step 5.
Step 8. Accept the tentative output address as an output address if it is less than Nturbo; otherwise, discard it.
Step 9. Increment the counter and repeat Steps 3 through 8 until all Nturbo interleaver output addresses are obtained.

Turbo Interleaver Parameter

Physical Layer Packet Size	Turbo Interleaver Block Size Nturbo	Turbo Interleaver Parameter
256	250	3
512	506	4
1024	1018	5
2048	2042	6
3072	3066	7
4096	4090	7

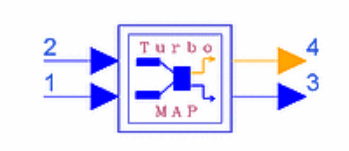
Turbo Interleaver Lookup Table Definition

Table Index	n=3 Entries	n=4 Entries	n=5 Entries	n=6 Entries	n=7 Entries
0	1	5	27	3	15
1	1	15	3	27	127
2	3	5	1	15	89
3	5	15	15	13	1
4	1	1	13	29	31
5	5	9	17	5	15
6	1	9	23	1	61
7	5	15	13	31	47
8	3	13	9	3	127
9	5	15	3	9	17
10	3	7	15	15	119
11	5	11	3	31	15
12	3	15	13	17	57
13	5	3	1	5	123
14	5	15	13	39	95
15	1	5	29	1	5
16	3	13	21	19	85
17	5	15	19	27	17
18	3	9	1	15	55
19	5	3	3	13	57
20	3	1	29	45	15
21	5	3	17	5	41
22	5	15	25	33	93
23	5	1	29	15	87
24	1	13	9	13	63
25	5	1	13	9	15
26	1	9	23	15	13
27	5	15	13	31	15
28	3	11	13	17	81
29	5	3	1	5	57
30	5	15	13	15	31
31	3	5	13	33	69

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_TurboMAPDecoder



Description: MAP decoder for turbo decoder
Library: 1xEV, Channel Coding
Class: SDF1xEV_TurboMAPDecoder

Parameters

Name	Description	Default	Symbol	Unit	Type	Range
PacketLength	output packet length (not including 6 tail bits)	250	N		int	{250,506,1018,2042,3066,4090}
CodeRate	code rate of turbo code: CodeRate1/2, CodeRate1/3, CodeRate1/4, CodeRate1/5	CodeRate1/2			enum	

Pin Inputs

Pin	Name	Description	Signal Type
1	D_In	input data	real
2	PriIn	priori value	real

Pin Outputs

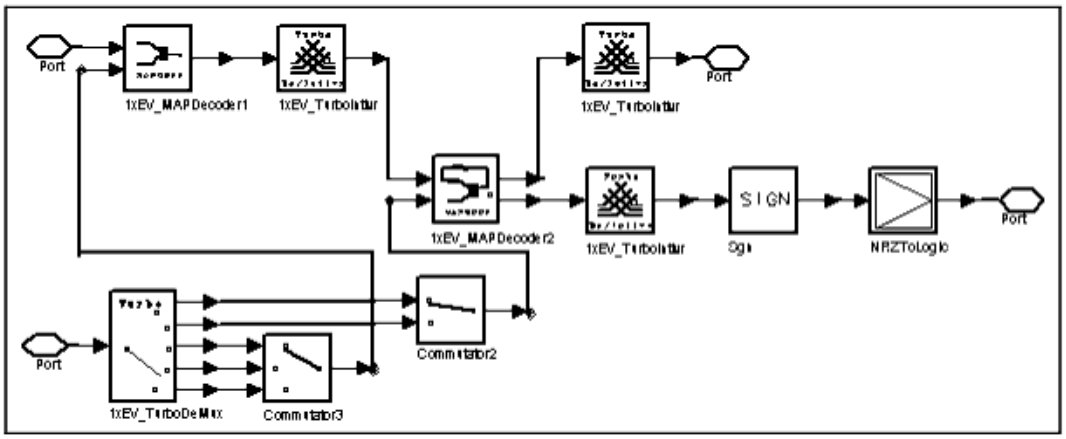
Pin	Name	Description	Signal Type
3	PriOut	priori value for next decoder	real
4	BitOut	decoded bits	int

Notes/Equations

1. This subnetwork is used to implement parallel concatenated MAP decoder for turbo code. The schematic for this subnetwork is shown in the following figure, which includes 1xEV_MAPDecoder1, 1xEV_MAPDecoder2 and turbo interleaver.

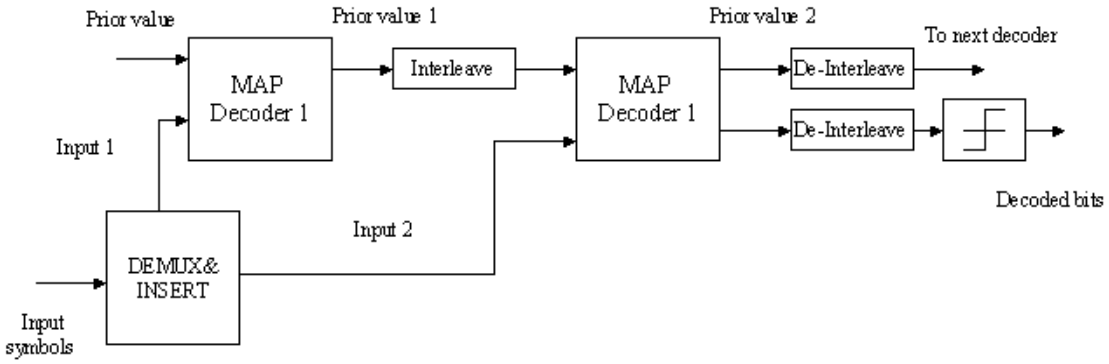
   This subnetwork can be used to construct an arbitrary level decoder to meet performance demands or the designer's iterative convergence criterion.

   The signal polluted by the channel noise is input at pin D_In and the decoded signal is output at pin BitOut. PriOut output is the a priori value for the next decoder used in a multi-level iterative decoder.



1xEV_TurboMAPDecoder Schematic

2. The following figure illustrates the turbo code decoder (MAP) structure. The first block MAP Decoder calculates the log-likelihood ratio (LLR) according to the a priori information and signal polluted by the channel noise using the BCJR algorithm [2]. The second block MAP Decoder calculates the log-likelihood ratio (LLR) according to the interleaved LLR from the block first MAP Decoder and the parity signal polluted by channel noise using the BCJR algorithm. Passing the sign sequence of the LLR output from the second block MAP Decoder through a NRZtoLogic model (which maps 1 to 0 and -1 to 1) and a de-interleaver obtains the decoded signal.



Turbo Code Decoder (MAP) Structure

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.
2. L.R. Bahl, J. Cocke, F. Jeinek and J. Raviv. "Optimal decoding of linear codes for minimizing symbol error rate," *IEEE Trans. Inform* . Theory, vol. IT-20. pp.248-287, Mar. 1974.
3. C.Berrou, A.Glavieux, and P. Thitimjshima, "Near Shannon limit error correcting coding: Turbo codes," *IEEE International Conference on Communications* , pp. 1064-1070, May 1993.

1xEV_TurboRSCEncoder

Description: RSC Encoder
Library: 1xEV, Channel Coding
Class: SDF1xEV_TurboRSCEncoder

Parameters

Name	Description	Default	Symbol	Unit	Type	Range
PacketLength	input packet length including 6 tail bits	256	N		int	{256,512,1024,2048,3072,4096}

Pin Inputs

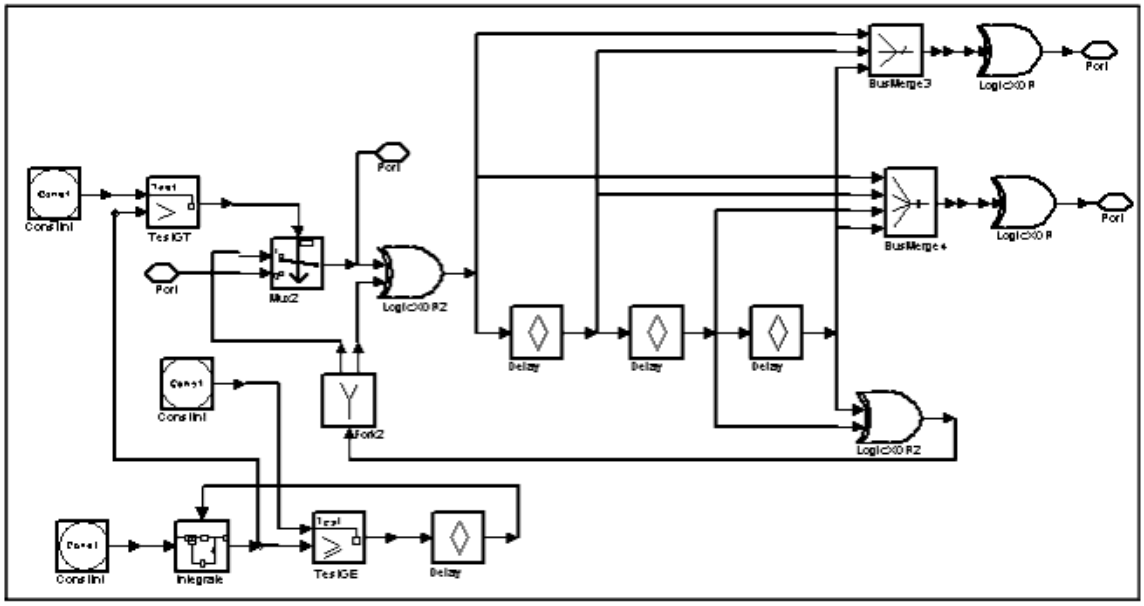
Pin	Name	Description	Signal Type
1	D_In	input data	int

Pin Outputs

Pin	Name	Description	Signal Type
2	X_Out	output data X	int
3	Y0_Out	output data Y0	int
4	Y1_Out	output data Y1	int

Notes/Equations

1. This subnetwork implements the recursive systematic convolutional (RSC) code encoder. The schematic for this subnetwork is shown in the following figure.



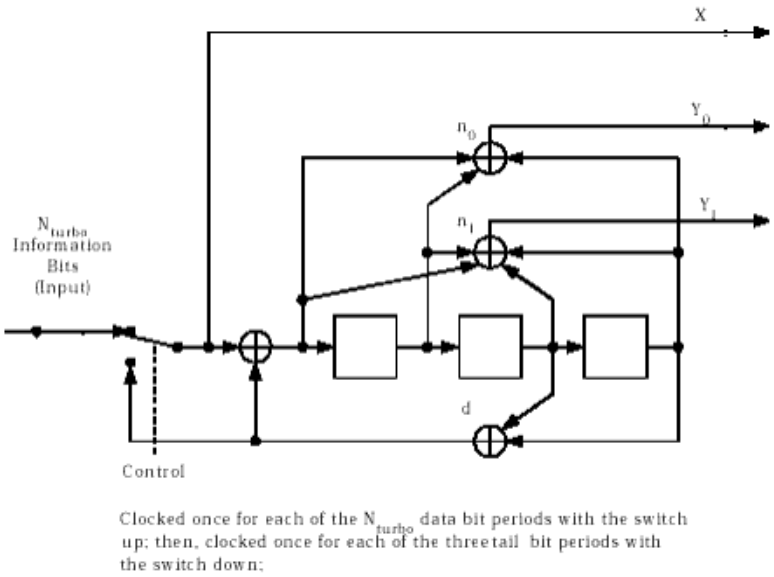
1xEV_TurboRSCEncoder Schematic

2. The transfer function for the constituent code is

$$G(D) = [1, \frac{n_0(D)}{d(D)}, \frac{n_1(D)}{d(D)}]$$

where d(D) = 1 + D2 + D3, n0(D) = 1 + D + D3, and n1(D) = 1 + D + D2 + D3.

The constituent encoder generates an output symbol sequence that is identical to the one generated by the encoder illustrated in the following figure. Initially, the states of the constituent encoder registers are set to zero.



RSC Encoder

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

Mobile Station Receiver Design Examples for 1xEV Design Library

Introduction

The MS_RX_wrk workspace shows 1xEV mobile station receiver measurements, including receiver sensitivity and dynamic range, single-tone desensitization, intermodulation spurious response attenuation, adjacent channel selectivity, and reverse traffic channel demodulation performance. Designs for these measurements include:

- MS_RxAdjacentSelectivity for mobile station receiver adjacent channel selectivity
- MS_RxDemodAWGN for forward traffic channel demodulation performance
- MS_RxDnmcRng for mobile station receiver sensitivity and dynamic range
- MS_RxIntermodulation for mobile station receiver intermodulation spurious response attenuation
- MS_RxSingleTone for mobile station receiver single-tone desensitization

Designs under this workspace consist of:

- BS signal source in baseband. 1xEV_FwdSrc provides the downlink signal source of different modulation scheme and data rates.
- Transmit modulation and up-convertor. The data source of baseband output from 1xEV_FwdSrc is up-converted to IF signal with RF_Mod_FIR, then modulated into RF signal with RF_TX_IFin1.
- Channel loss and interfering signal combination. The transmitted RF signal is then attenuated by RF channel (GainRF model) and combined with interfering signals (modulated or continuous waveform) at given frequency offsets.
- Down-convertor and demodulation. At the receiver side, the received signal is demodulated to be the baseband signal by RF_RX_IFout1 and RF_Demod_FIR models.
- Mobile station receiver in baseband. CDMA2K_FwdReceiver is used to demodulate the received baseband signals.

Intermodulation Spurious Response Attenuation

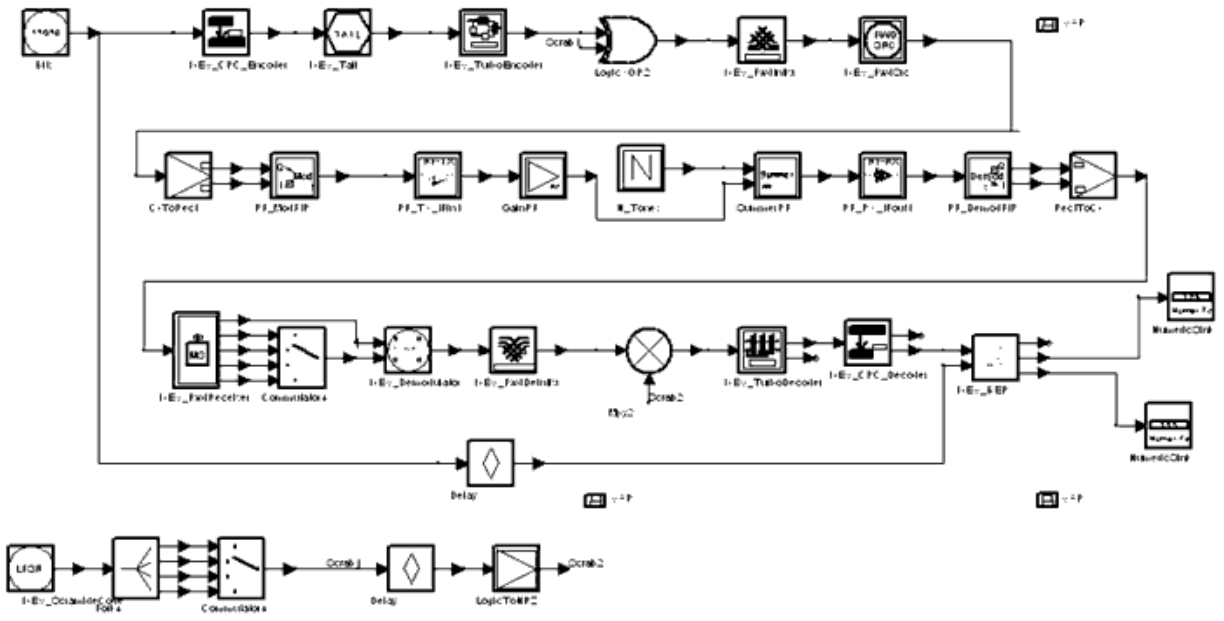
MS_RxIntermodulation

Features

- Forward pilot and traffic channel
- $\hat{I}_{or}$
  is -102.4 dBm/1.23 MHz; tone powers are −40 dBm; tone offset 1 is 900 kHz; tone offset 2 is 1700 kHz
- FER and BER of traffic channel measurements

Description

This example verifies a receiver's ability to receive an IS-856 signal on its assigned channel frequency in the presence of two interfering CW tones as defined in section 3.1.1.3.3 of 3GPP2 C.S0033. The schematic for this design is shown in the figure below.



MS_RxIntermodulation Schematic

Simulation Results

Simulation results displayed in MS_RxIntermodulation.dds are shown in the figure below.

Conditions:

Ior_dBm	TonePower_dBm	ToneOffset1_MHz	ToneOffset2_MHz
-102.400	-40.000	0.900	1.700

Ior in receiving end is -102.3dBm

Tone 1:
Frequency offset +900KHz
Power: -40dBm

Tone2:
Frequency offset +1700KHz
power: -40dBm

Expected:

less than 1% within 95%Confidence

Result:

var("1xEV_PER")
0.000

Eqn Ior_dBm=real(Ior)

Eqn TonePower_dBm=real(TonePower)

Eqn ToneOffset1_MHz=real(ToneOffset1)

Eqn ToneOffset2_MHz=real(ToneOffset2)

.

PER performance with Intermodulation Spurious Response Attenuation

Benchmark

- Hardware Platform: Pentium III 1000 MHz, 512 MB memory
- Software Platform: Windows 2000, ADS 2001
- Data Points: 300 packets
- Simulation Time: approximately 23 minutes

Single-Tone Desensitization

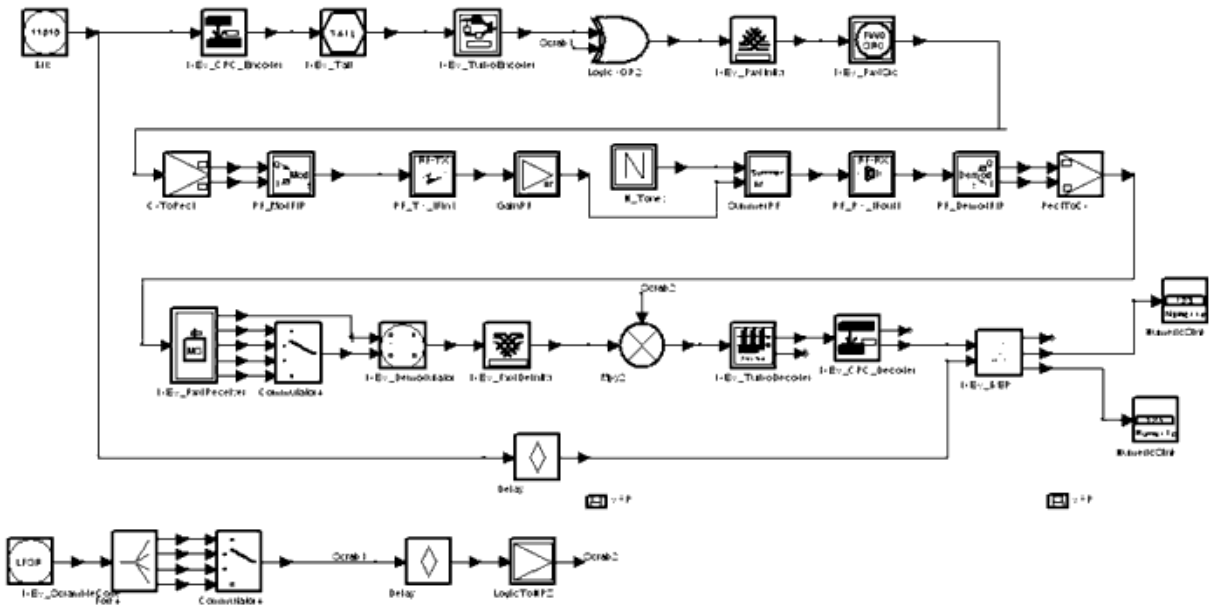
MS_RxSingleTone

Features

- Forward pilot and traffic channel
- $\hat{I}_{or}$
  is -102.4 dBm/1.23 MHz; tone power is −30 dBm; tone offset is 900 kHz
- FER and BER of traffic channel measurements

Description

This example verifies a receiver's ability to receive an IS-856 signal at its assigned channel frequency in the presence of a single tone spaced at a given frequency offset from the center frequency of the assigned channel as defined in section 3.1.1.3.2 of 3GPP2 C.S0033. The schematic for this design is shown in the following figure.



MS_RxSingleTone Schematic

Simulation Results

Simulation results displayed in MS_RxSingleTone.dds are shown in the following figure.

Conditions:

Ior_dBm	TonePower_dBm	ToneOffset_MHz
-102.400	-30.000	0.900

Ior in receiving end is -102.3dBm
Tone 1:
Frequency offset +900KHz
Power: -30dBm

Eqn Ior_dBm=real(Ior)

Eqn TonePower_dBm=real(TonePower)

Eqn ToneOffset_MHz=real(ToneOffset)

Expected:
less than 1% within 95%Confidence

Result:

var("1xEV_PER")
0.000

Single-Tone Desensitization Simulation Results

Benchmark

- Hardware Platform: Pentium III 1000 MHz, 512 MB memory
- Software Platform: Windows 2000, ADS 2001
- Data Points: 300 packets
- Simulation Time: approximately 21 minutes

Adjacent Channel Selectivity

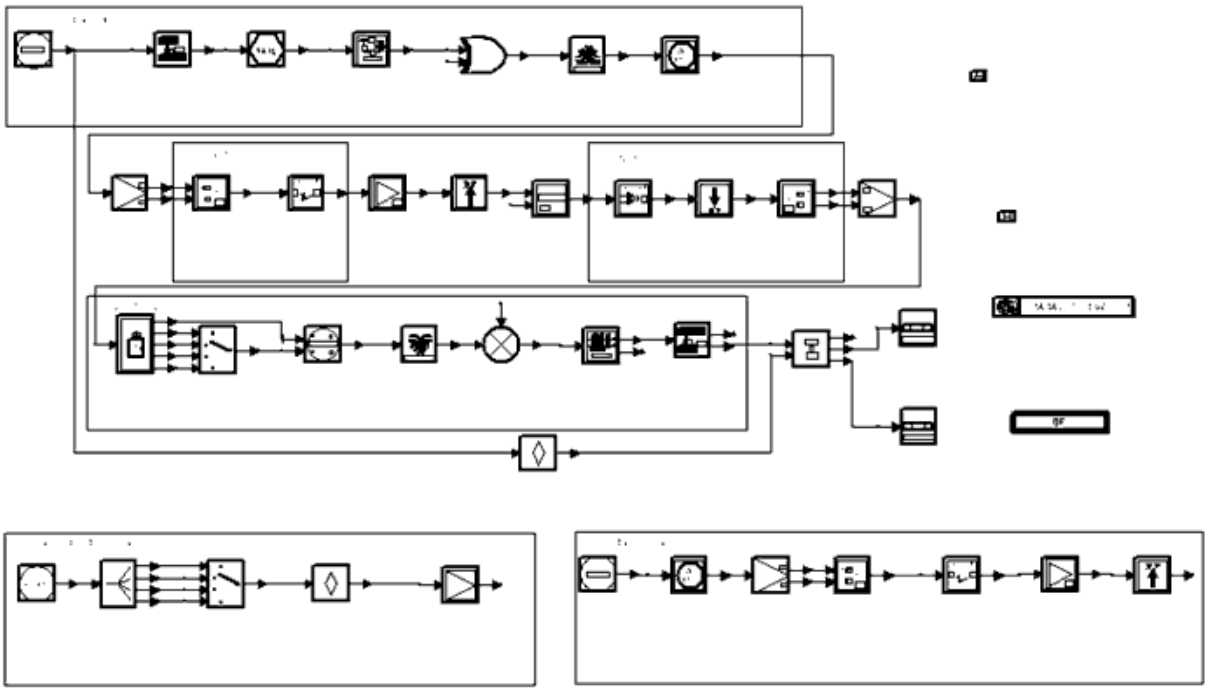
MS_RxAdjacentSelectivity

Features

- Forward traffic channel data rate is 307.2 kbps in 2-slot version
- $\hat{I}_{or}$
  is -102.4 dBm/1.23 MHz
- Applies to band class 6 mobile stations only
- PER of fundamental channel measurement

Description

This example measures the receiver adjacent channel selectivity, as defined in section 3.1.1.3.4 of 3GPP2 C.S0033. PER is measured in the presence of another CDMA signal that is offset from the center frequency of the assigned channel by +2.5 or −2.5 MHz. The schematic for this design is shown in the following figure.



MS_RxAdjacentSelectivity Schematic

Simulation Results

Simulation results displayed in MS_RxAdjacentSelectivity.dds are shown in the following figure.

Conditions:

Iorr_dBm
-102.400

Eqn Iorr_dBm=real(Iorr)

In Test Case 1, the adjacent channel offset from the the carrier is +2.5MHz, while in Test Case 2, the offset is -2.5MHz.

Expected: less than 1% within 95%Confidence

Result:

Index	var("1xEV_PER")	
	TestCase=1.000	TestCase=2.000
500	0.000	0.000

Adjacent Channel Selectivity Performance

Benchmark

- Hardware Platform: Pentium III 800 MHz, 512 MB memory
- Software Platform: Windows NT4.0, ADS 2001
- Data Points: 500 packets
- Simulation Time: approximately 3.5 hours

Forward Traffic Channel Demodulation

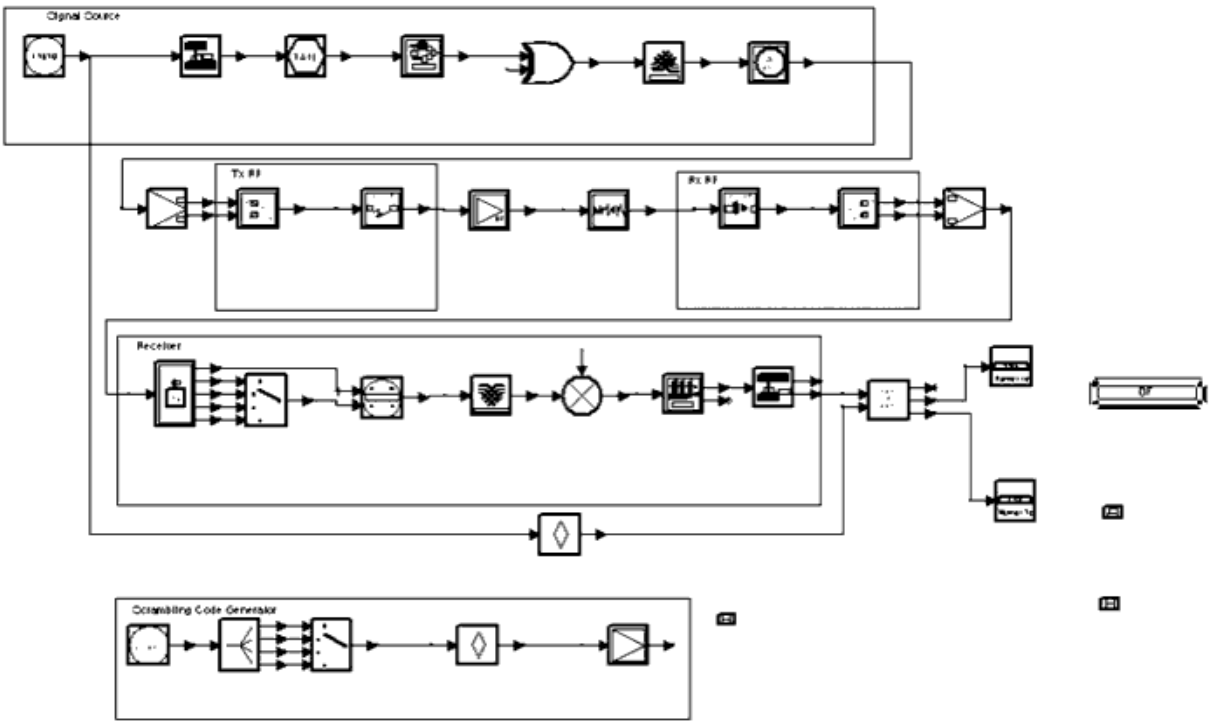
MS_RxDemodAWGN

Features

- Forward Traffic Channel data rate is 614.4 kbps in 1-slot version
- $\hat{I}_{oc}$
  is -55. 6 dBm/1.23 MHz; $\hat{I}_{or}/I_{oc}$
  is 0.6 dB
- PER of fundamental channel measurements

Description

This example verifies the demodulation performance of forward traffic channel under AWGN conditions, as defined in section 3.1.1.2.1 of 3GPP2 C.S0033. The schematic for this design is shown in the following figure.



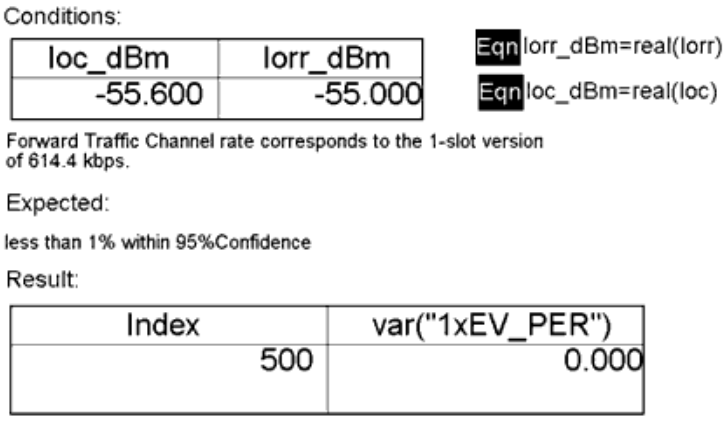
MS_RxDemodAWGN Schematic

Notes

Designers can set up system parameters or replace a component according to their particular requirements.

Simulation Results

Simulation results displayed in MS_RxDemodAWGN.dds are shown in the following figure.


Conditions:

Ioc_dBm	Iorr_dBm
-55.600	-55.000

Eqn Iorr_dBm=real(Iorr)

Eqn Ioc_dBm=real(Ioc)

Forward Traffic Channel rate corresponds to the 1-slot version of 614.4 kbps.

Expected:

less than 1% within 95%Confidence

Result:

Index	var("1xEV_PER")
500	0.000

Forward Traffic Channel Demodulation Performance (AWGN)

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 M memory
- Software Platform: Windows NT4.0, ADS2001
- Data Points: 500 packets
- Simulation Time: approximately 3.5 hours

Receiver Sensitivity and Dynamic Range

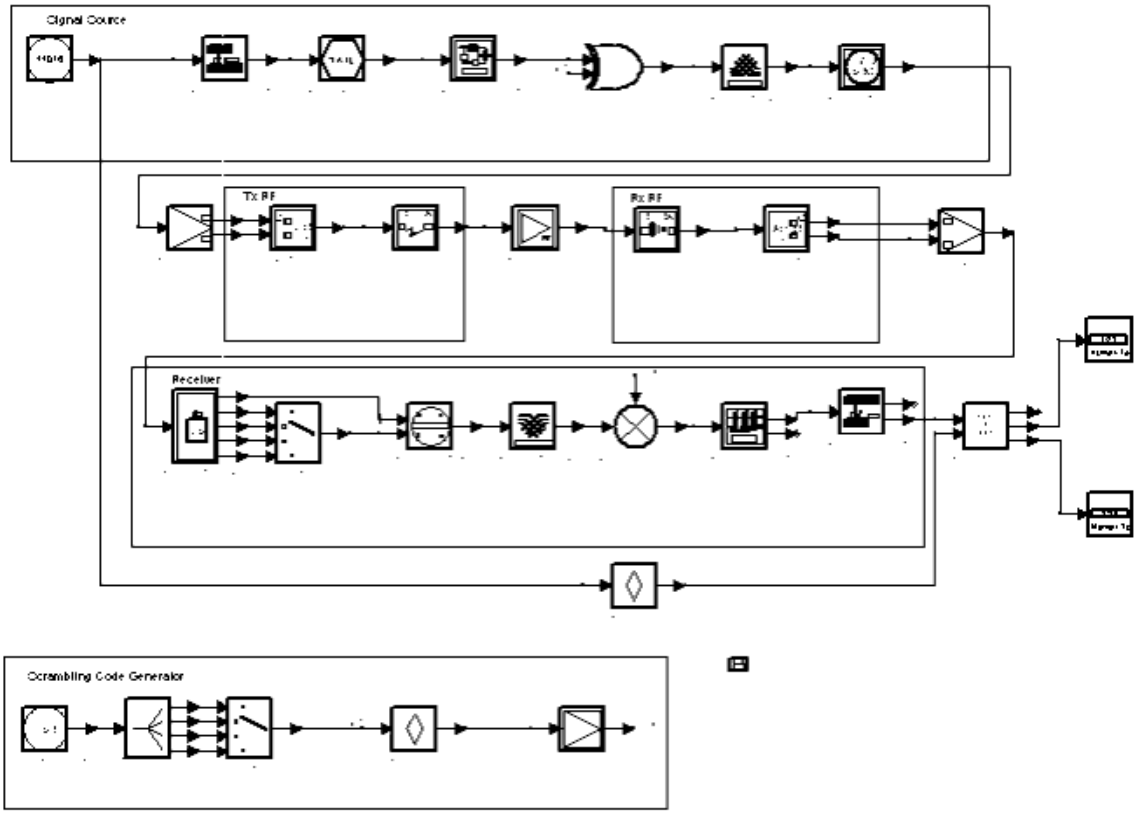
MS_RxDnmcRng

Features

- Forward Traffic Channel Data Rate is 307.2 kbps in 2-slot version
- $\hat{I}_{or}$
  is -105.5 dBm/1.23 MHz
- PER of fundamental channel measurements

Description

This example verifies the receiver sensitivity and dynamic range, as defined in section 3.5.1 of 3GPP2 C.S0033. The schematic for this design is shown in the following diagram.



MS_RxDnmcRng Schematic

Notes

Receiver sensitivity and dynamic range can be measured using this design. The dynamic range can be measured by changing signal power at the receiver side.

Simulation Results

Simulation results displayed in MS_RxDnmcRng.dds are shown in the following diagram.

Conditions:

Iorr_dBm
-105.500

Eqn Iorr_dBm=real(Iorr)

Forward Traffic Channel rate corresponds to the 2-slot version of 307.2 kbps.

Expected:

less than 0.5% within 95%Confidence

Result:

Index	var("1xEV_PER")
1000	0.000

Receiver Sensitivity and Dynamic Range Simulation Results

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT 4.0 Workstation, ADS2001
- Data Points: 1000 frames.
- Simulation Time: approximately 3.5 hours

References

1. 3GPP2 C.S0033, *Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Terminal* , Proposed Publication Version, December 7, 2001.

Mobile Station Transmitter Design Examples for 1xEV Design Library

Introduction

The MS_Tx_wrk workspace shows 1xEV mobile station transmitter characteristics, including waveform quality (rho), RF output power, code domain power, conducted spurious emissions and occupied bandwidth. Designs for these include:

- MS_TxACPR for Adjacent Channel Power Ratio measurement
- MS_TxCDP for Code Domain Power measurements
- MS_TxPower for RF output power measurements
- MS_TxRho for waveform quality measurement
- MS_TxSpectrum for conducted spurious emissions and occupied bandwidth measurements

Adjacent Channel Power Ratio

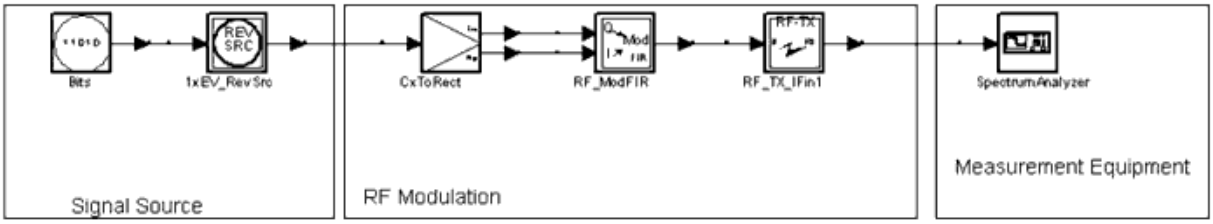
MS_TxACPR

Features

- ACPR is measured by SpectrumAnalyzer component
- Pilot, DRC , ACK, and Data channels are enabled

Description

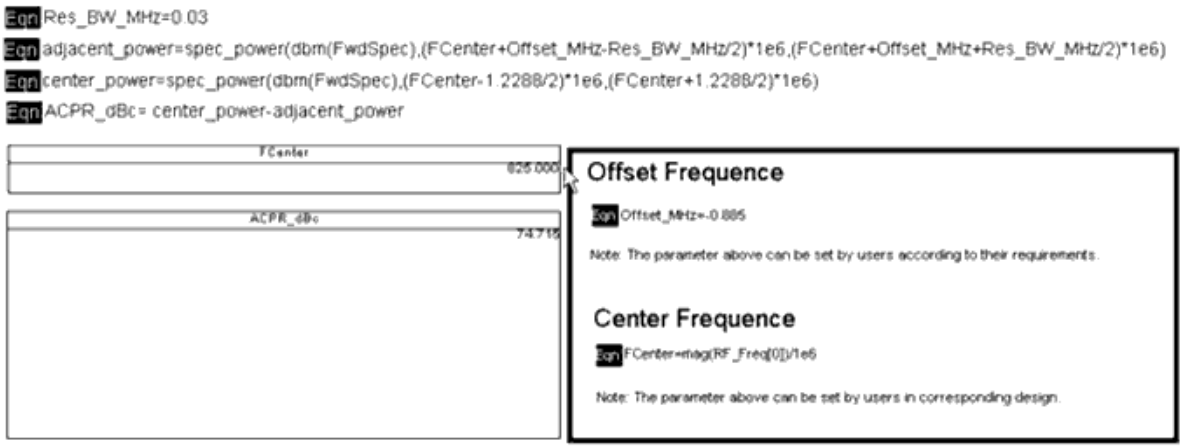
This example measures ACPR for 1xEV reverse link. The schematic for this design is shown in the following figure. 1xEV_RevSrc generates the baseband signal that is up-converted to an IF signal with RF_ModFIR, then modulated into an RF signal with RF_TX_IFin1 for measurement. The SpectrumAnalyzer component implements spectrum measurement.



MS_TxACPR Schematic

Simulation Results

Simulation results are shown in the following figure.



ACPR for 1xEV Reverse Link

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB
- Software Platform: Windows NT Workstation 4.0, ADS 2002
- Simulation Time: approximately 3 minutes

References

1. 3GPP2 C.S0033, *Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network* , Initial Revision, Aug. 24, 2001.

Code Domain Power

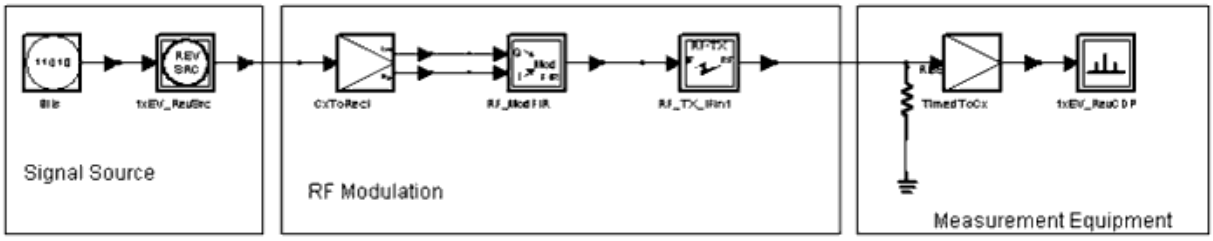
MS_TxCDP

Features

- Code domain power is measured by a CDP meter
- DRC, ACK, and Data channel output power are tested in three cases respectively

Description

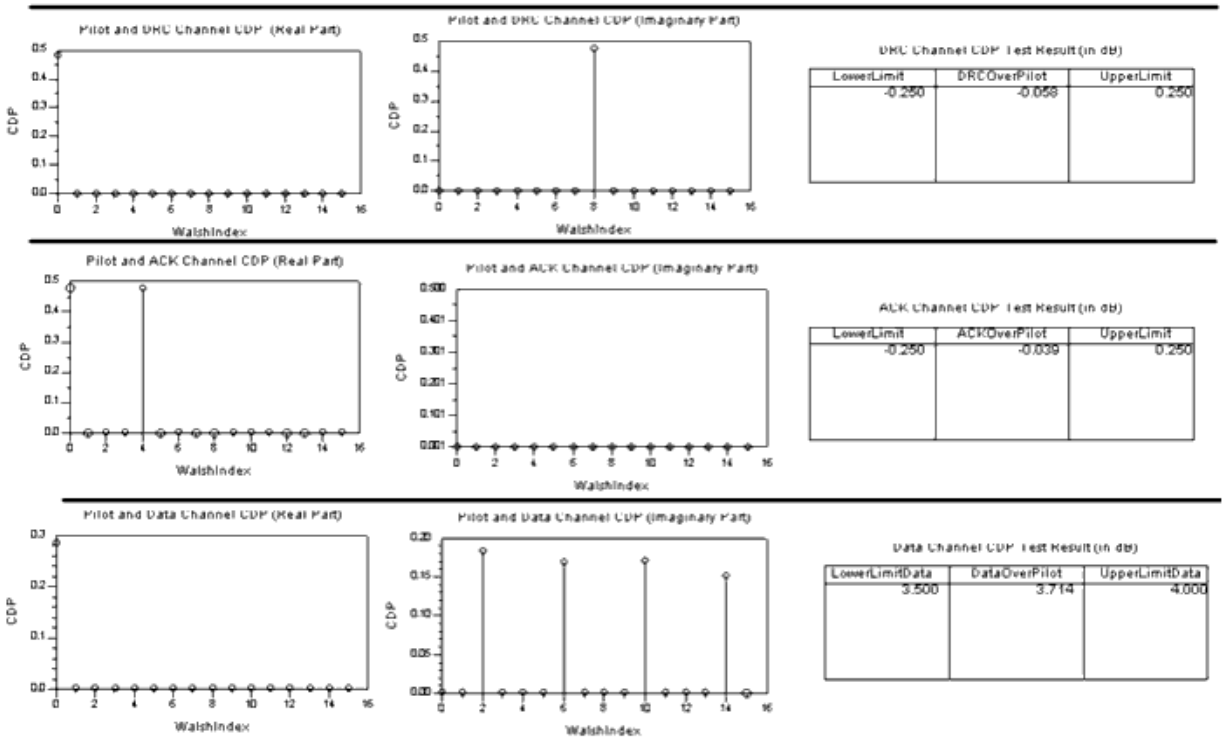
This example measures code domain power for 1xEV reverse link. Code domain power is the power in each code channel of a CDMA system. The schematic for this design is shown in the following figure. 1xEV_RevSrc generates the baseband signal that is up-converted to an IF signal with RF_ModFIR, then modulated into an RF signal with RF_TX_IFin for measurement. 1xEV_RevCDP implements the code domain power measurement.



MS_TxCDP Schematic

Simulation Results

Simulation results are shown in the following figure. The CDP value of DRC Channel over Pilot channel shall be within DRCChannelGain 0.25 dB. The CDP value of ACK Channel over Pilot channel shall be within ACKChannelGain 0.25 dB. The CDP value of Data Channel over Pilot channel shall be within DataChannelGain 0.25 dB.



Code Domain Power for 1xEV Reverse Link

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 2002
- Simulation Time: approximately 2 minutes

References

1. 3GPP2 C.S0033, *Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network* , Initial Revision, Aug. 24, 2001.

RF Output Power

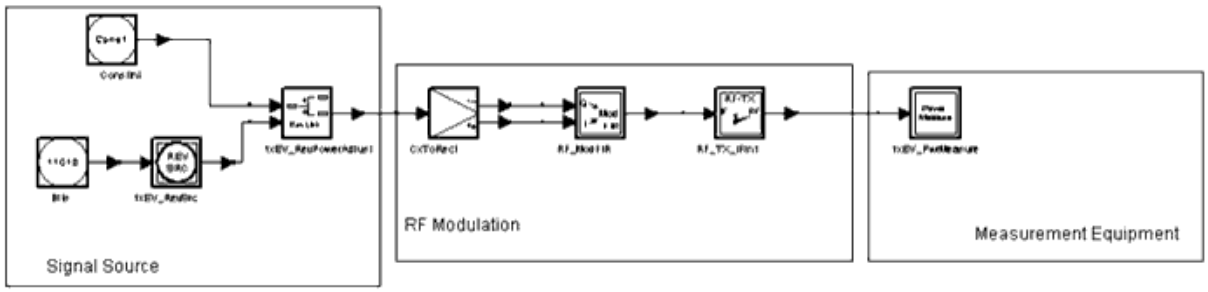
MS_TxPower

Features

- RF output power is measured with a power meter
- Pilot Channel, DRC Channel, ACK Channel and Data Channel are enabled.
- Open loop power control is enabled

Description

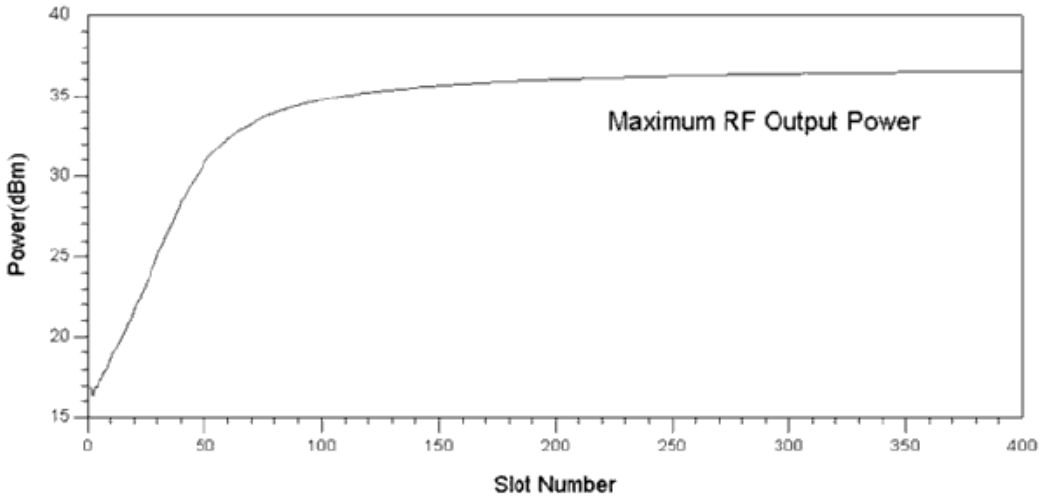
This example measures the RF output power of mobile station. When the power is measured, continuous 0s are sent as the power control bits to obtain the maximum output power. The schematic for this design is shown in the following figure. 1xEV_RevSrc generates the baseband signal that is up-converted to an IF signal with RF_ModFIR then modulated into an RF signal with RF_TX_IFin1 for measurement. 1xEV_PwrMeasure implements the power measurement.



MS_TxPower Schematic

Simulation Results

Simulation results are shown in the following figure.



Transmit Power Measurement for 1xEV Reverse Link

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 2002
- Simulation Time: approximately 8 minutes

References

1. 3GPP2 C.S0033, *Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network* , Initial Revision, Aug. 24, 2001.

Waveform Quality

MS_TxRho

Features

- Waveform quality factor Rho is measured with a Rho meter
- Pilot Channel, DRC Channel, ACK Channel and Data Channel are enabled.

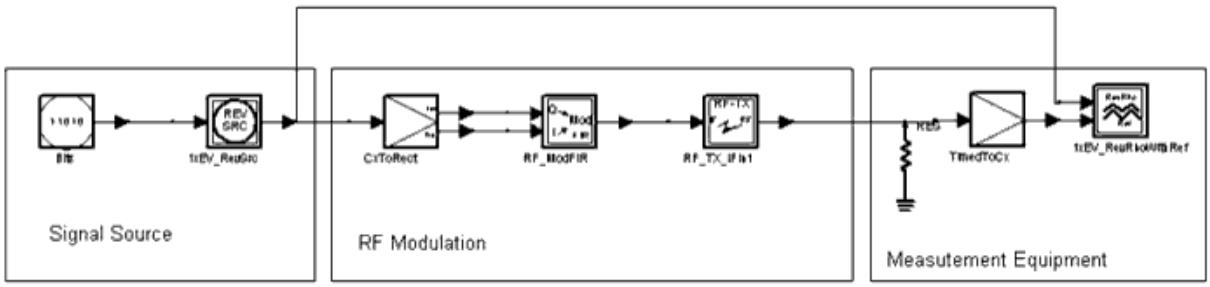
Description

This example is used to measure the waveform quality for 1xEV reverse link. Waveform quality is measured by determining the normalized correlated power between the actual and the ideal waveform.

The schematic for this design is shown in the following figure. 1xEV_RevSrc generates the baseband signal that is up-converted to an IF signal with RF_ModFIR, then modulated into an RF signal with RF_TX_IFin1 for measurement. 1xEV_RevRhoWithRef implements the Rho measurements.

The two data paths from the source to the measurement component are:

- one for the real transmitted signal that goes through RF modulation;
- one for the reference signal used in the measurement.



MS_TxRho Schematic

Simulation Results

Simulation results are shown in the following figure.

Rho
0.9862

Rho Measurement for 1xEV Reverse Link

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 2002
- Simulation Time: approximately 2 minutes

References

1. 3GPP2 C.S0033, *Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network* , Initial Revision, Aug. 24, 2001.

Transmit Spectrum and Occupied Bandwidth

MS_TxSpectrum

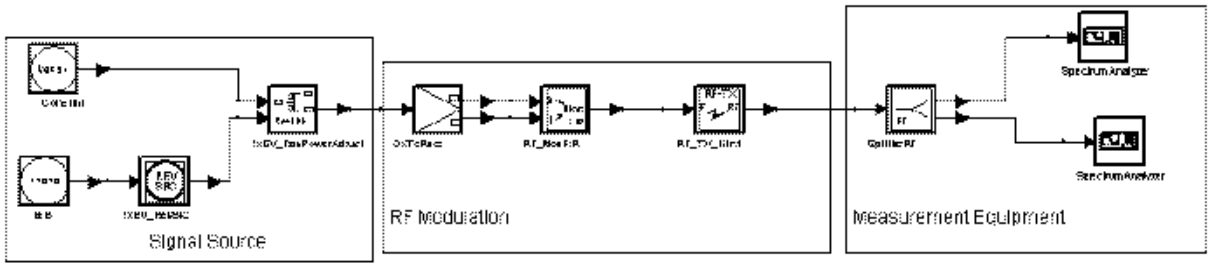
Features

- Conducted spurious emissions and occupied bandwidth are measured with a SpectrumAnalyzer component
- Pilot Channel, DRC Channel, ACK Channel and Data Channel are enabled

Description

This example measures conducted spurious emissions and occupied bandwidth of 1xEV reverse link. Conducted spurious emissions are emissions at frequencies that are outside the assigned CDMA Channel, measured at the sector RF output port. Occupied bandwidth is the frequency range, whereby the power of emissions averaged over the frequency above and under the edge frequency are 0.5% each of the total radiation power of a modulated carrier.

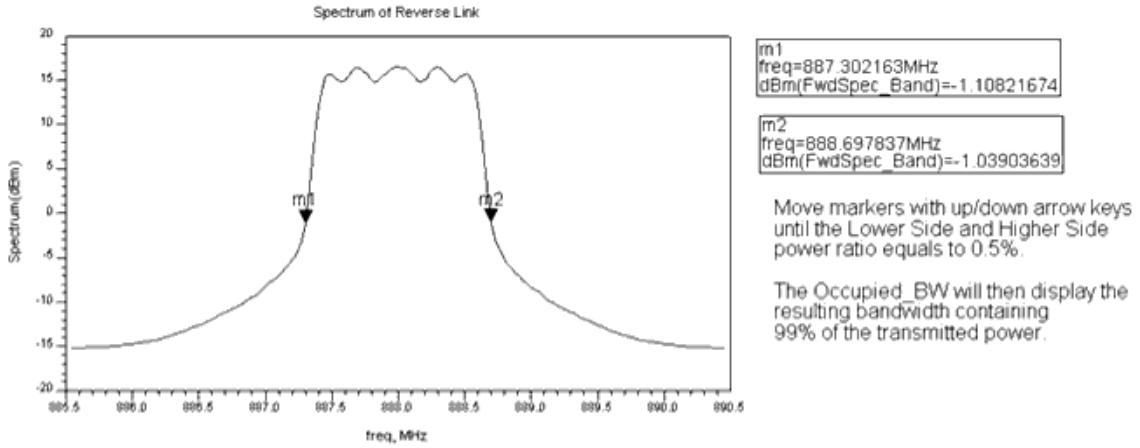
The schematic for this design is shown in the following figure. 1xEV_RevSrc generates the baseband signal that is up-converted to IF signal with RF_ModFIR, then modulated into an RF signal with RF_TX_IFin1 for measurement. SpectrumAnalyzer implements the spectrum measurement.



MS_TxSpectrum Schematic

Simulation Results

Simulation results are shown in the following two figures. The *Equations* page shows the equations that are used for calculating the spectrum. The occupied bandwidth test applies to band class 3 and 6 only; band class 3 is used in the example design and thresholds are set according to Section 3.1.2.4.1 and 3.1.2.4.4, reference[1]. If other band classes are used, the thresholds in the *Equations* page should be changed accordingly. Comparison results for conducted spurious emissions are displayed in each page as *Passed* or *Failed* .



m1
freq=887.302163MHz
dBm(FwdSpec_Band)=-1.10821674

m2
freq=888.697837MHz
dBm(FwdSpec_Band)=-1.03903639

Move markers with up/down arrow keys until the Lower Side and Higher Side power ratio equals to 0.5%.

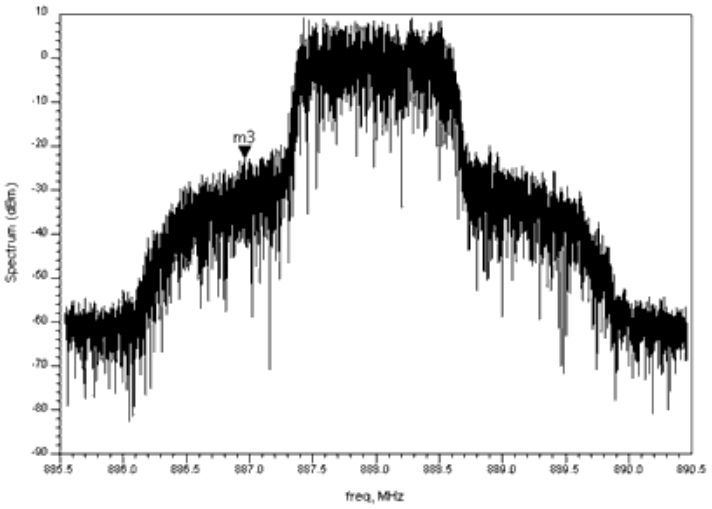
The Occupied_BW will then display the resulting bandwidth containing 99% of the transmitted power.

Lower_Side_percentage	Higher_Side_percentage	Total_Power_W
0.405514	0.410882	1.455613

Occupied_BandWidth_MHz
1.396

The occupied channel bandwidth shall be less than 1.48MHz based on a chip rate of 1.2288Mcps.
The resolution bandwidth of the spectrum analyzer is 30kHz

Occupied Bandwidth for 1xEV Reverse Link



Move marker with left/right arrow keys or mouse to the frequency you are interested in to find whether the transmitter emission in 30KHz at that frequency is within the limitaion specified in section 3.1.2.4.1, 3GPP2 C.S0033.

Band Class used in the example design is 3, the standard can be changed by users in the page titled 'Equations' according to their requirement for Band Class.

P30K_dBc	P30K_dBm
-45.817	-14.187

m3
freq=886.960746MHz
dBm(FwdSpec_Emission)=-22.90649457

The test result for the transmitter emission within 30KHz at this frequency is Passed

Conducted Spurious Emission for 1xEV Reverse Link

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 2002
- Simulation Time: approximately 5 minutes

References

1. 3GPP2 C.S0033, *Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network* , Initial Revision, Aug. 24, 2001.

Modems for 1xEV Design Library

- *1xEV 8PSKMod* (1xev)
- *1xEV 16QAMMod* (1xev)
- *1xEV BaseFilter* (1xev)
- *1xEV BiWalshCode* (1xev)
- *1xEV Demodulator* (1xev)
- *1xEV FwdDeTDM* (1xev)
- *1xEV FwdTDM* (1xev)
- *1xEV HPSK* (1xev)
- *1xEV LgPNCode* (1xev)
- *1xEV MAC TDM* (1xev)
- *1xEV Modulator* (1xev)
- *1xEV PhaseEqualizer* (1xev)
- *1xEV PNCode* (1xev)
- *1xEV QPSK* (1xev)
- *1xEV RateDematch* (1xev)
- *1xEV RateMatch* (1xev)
- *1xEV RevPowerAdjust* (1xev)
- *1xEV ScrambleCode* (1xev)
- *1xEV SimplexEncoder* (1xev)
- *1xEV WalshCode* (1xev)
- *1xEV WalshCover* (1xev)
- *1xEV WalshModulator* (1xev)

1xEV_8PSKMod

Description: Generation of 8PSK modulated signal
Library: 1xEV, Modems
Class: SDF1xEV_8PSKMod

Pin Inputs

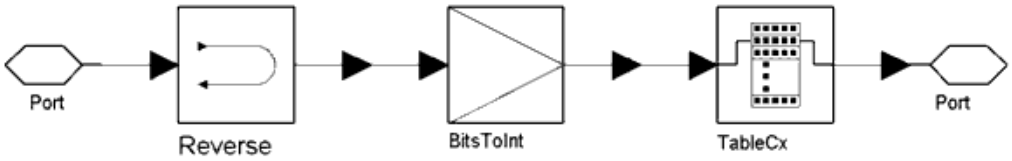
Pin	Name	Description	Signal Type
1	input	input bits, taking the value of 0 or 1	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	complex envelope of modulated signal	complex

Notes/Equations

1. This subnetwork is used to generate an 8PSK modulated signal. The schematic for this subnetwork is shown in the following figure; it includes Reverse, BitsToInt and TableCx models.



Structure of 1xEV_8PSKMod

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_16QAMMod

Description: Generation of 16QAM modulated signal
Library: 1xEV, Modems
Class: SDF1xEV_16QAMMod

Pin Inputs

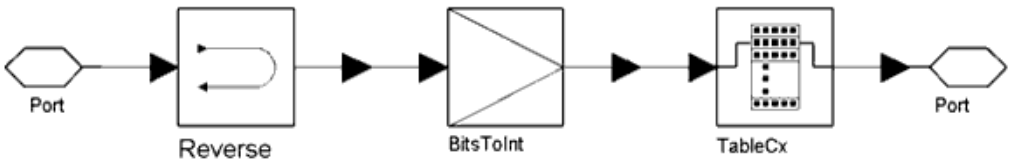
Pin	Name	Description	Signal Type
1	input	input bits, taking the value of 0 or 1	int

Pin Outputs

Pin	Name	Description	Signal Type
2	output	complex envelope of modulated signal	complex

Notes/Equations

1. This subnetwork is used to generate a 16QAM signal. The schematic for this subnetwork is shown in the following figure.

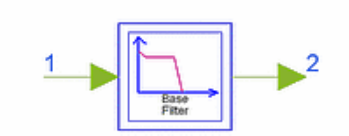


Structure of 1xEV_16QAMMod

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_BaseFilter



Description: Complex FIR baseband filter for 1xEV system
Library: 1xEV, Modems
Class: SDF1xEV_BaseFilter

Pin Inputs

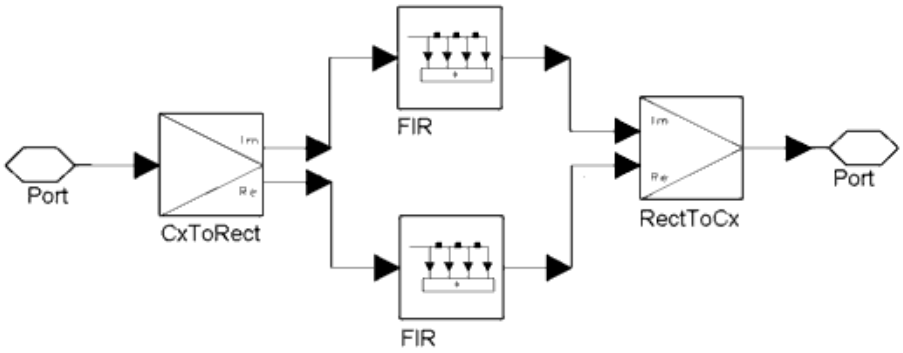
Pin	Name	Description	Signal Type
1	SigIn	input signal	complex

Pin Outputs

Pin	Name	Description	Signal Type
2	SigOut	output signal	complex

Notes/Equations

1. This subnetwork is used as a baseband filter. The schematic for this subnetwork is shown in the following figure.



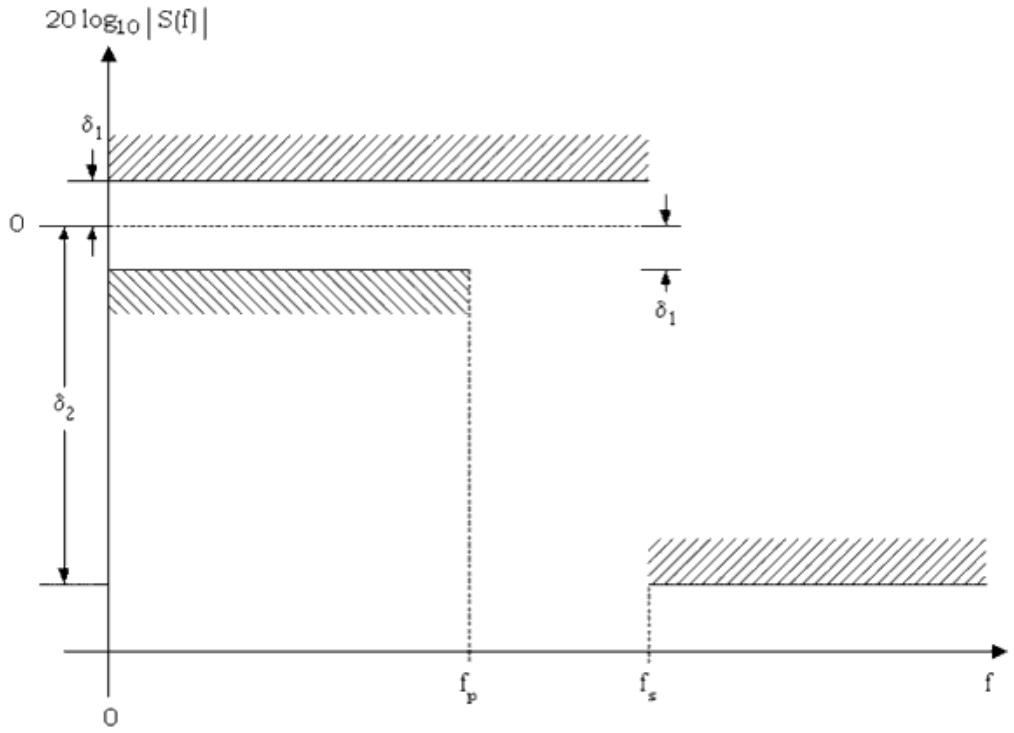
1xEV_BaseFilter Schematic

2. Baseband filters in 1xEV must have a frequency response S(f) that satisfies the limits given in the following figure. Specifically, the normalized frequency response of the filter must be contained within δ1 in the passband $0 \le f \le f_p$, and must be less than or equal to −δ2 in the stopband $f \ge f_s$. For SR1 the numerical values for the parameters are δ1 = 1.5 dB, δ2 = 40 dB, f_p = 590 kHz, and f_s = 740 kHz.

   Let s(t) be the impulse response of the baseband filter. Then s(t) should satisfy:

$$MeanSquaredError = \sum_{k=0}^{\infty} [\alpha S(kT_s - \tau) - h(k)]^2 \le 0.03$$

where the constants α and τ are used to minimize the mean squared error. The constant T_s is equal to 203.451... ns, which equals one quarter of the duration of a PN chip. The values of the coefficients h(k), for k < 48, are given in Table 9.3.1.3.5.1-1 listed in [1], h(k) = 0 for k>= 48. Note that h(k) equals h(47 - k).



Baseband Filter Frequency Response Limits

The coefficients of h(k) are listed in the following table.

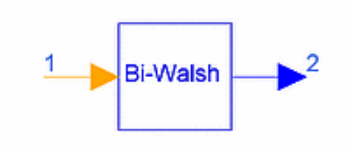
Coefficients of h(k)

k	h[k]
0,47	-0.025288315
1,46	-0.034167931
2,45	-0.035752323
3,44	-0.016733702
4,43	0.021602514
5,42	0.064938487
6,41	0.091002137
7,40	0.081894974
8,39	0.037071157
9,38	-0.021998074
10,37	-0.060716277
11,36	-0.051178658
12,37	0.007874526
13,34	0.084368728
14,33	0.126869306
15,34	0.094528345
16,31	-0.012839661
17,30	-0.143477028
18,29	-0.211829088
19,28	-0.140513128
20,27	0.094601918
21,26	0.441387140
22,25	0.785875640
23,24	1.0

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_BiWalshCode



Description: Bi-Walsh code generator
Library: 1xEV, Modems
Class: SDF1xEV_BiWalshCode

Parameters

Name	Description	Default	Symbol	Unit	Type	Range
WalshLength	length of Walsh code	64	N		int	2^n, n=1,...,11

Pin Inputs

Pin	Name	Description	Signal Type
1	Index	bi-Walsh code index	int

Pin Outputs

Pin	Name	Description	Signal Type
2	Walsh	Walsh code	real

Notes/Equations

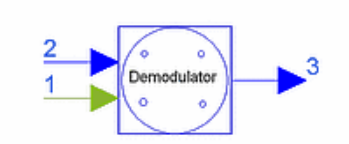
1. This model is used to generate a variable length bi-Walsh code sequence.
2. The bi-Walsh sequence is specified in terms of Walsh functions and their bit-by-bit complements by
   $W_{i/2}^{N/2}$ for i=0,2, ... , N
   $\overline{W}_{(i-1)/2}^{N/2}$ for i=1,3, ... , N

   where *i* =0, 1, ... , N is the bi-Walsh code index, *N* =2^n (n = 1, ... , 11) and $\overline{W}_i^{N/2}$ is the bit-by-bit complement of the Walsh function of order *i*.

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_Demodulator



Description: Demodulator for QPSK, 8PSK and 16QAM
Library: 1xEV, Modems
Class: SDF1xEV_Demodulator

Parameters

Name	Description	Default	Unit	Type	Range
DataRate	data rate of the forward traffic channel: R38.4kbps 16 slot, R76.8kbps 8 slot, R153.6kbps 4 slot, R307.2kbps 2 slot, R614.4kbps 1 slot, R307.2kbps 4 slot, R614.4kbps 2 slot, R1228.8kbps 1 slot, R921.6kbps 2 slot, R1843.2kbps 1 slot, R1228.8kbps 2 slot, R2457.6kbps 1 slot	R38.4kbps 16 slot		enum	
Decision	decision method of Turbo decoder: Soft decision, Hard decision	Soft decision		enum	

Pin Inputs

Pin	Name	Description	Signal Type
1	Input	input data from Rake receiver	complex
2	Pilot	input pilot data from Rake receiver	real

Pin Outputs

Pin	Name	Description	Signal Type
3	Output	output decision values	real

Notes/Equations

1. This model performs QPSK, 8PSK and 16QAM demodulation and provides soft-decision values for Viterbi or turbo decoders.
2. Each firing, 2 Output tokens for QPSK, 3 Output tokens for 8PSK and 4 Output tokens for 16QAM are produced when one Input token and one Pilot token are consumed. The Pilot input is used to estimate the signal strength only when 16QAM is demodulated.

Forward Traffic and Control Channel Modulation Parameters

Number of Values per Physical Layer Packet

Data Rate (kbps)	Slots	Bits	Modulation Type
38.4	16	1,024	QPSK
76.8	8	1,024	QPSK
153.6	4	1,024	QPSK
307.2	2	1,024	QPSK
614.4	1	1,024	QPSK
307.2	4	2,048	QPSK
614.4	2	2,048	QPSK
1,228.8	1	2,048	QPSK
921.6	2	3,072	8PSK
1,843.2	1	3,072	8PSK
1,228.8	2	4,096	16QAM
2,457.6	1	4,096	16QAM

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_FwdDeTDM

Description: Time division demultiplex for forward link
Library: 1xEV, Modems
Class: SDF1xEV_FwdDeTDM

Parameters

Name	Description	Default	Unit	Type	Range
DataRate1	data rate of the first packet in the forward traffic channel: RateA01, RateA02, RateA03, RateA04, RateA05, RateA06, RateA07, RateA08, RateA09, RateA10, RateA11, RateA12	RateA01		enum	
DataRate2	data rate of the second packet in the forward traffic channel: RateB01, RateB02, RateB03, RateB04, RateB05, RateB06, RateB07, RateB08, RateB09, RateB10, RateB11, RateB12	RateB01		enum	
DataRate3	data rate of the third packet in the forward traffic channel: RateC01, RateC02, RateC03, RateC04, RateC05, RateC06, RateC07, RateC08, RateC09, RateC10, RateC11, RateC12	RateC01		enum	
DataRate4	data rate of the fourth packet in the forward traffic channel: RateD01, RateD02, RateD03, RateD04, RateD05, RateD06, RateD07, RateD08, RateD09, RateD10, RateD11, RateD12	RateD01		enum	

Pin Inputs

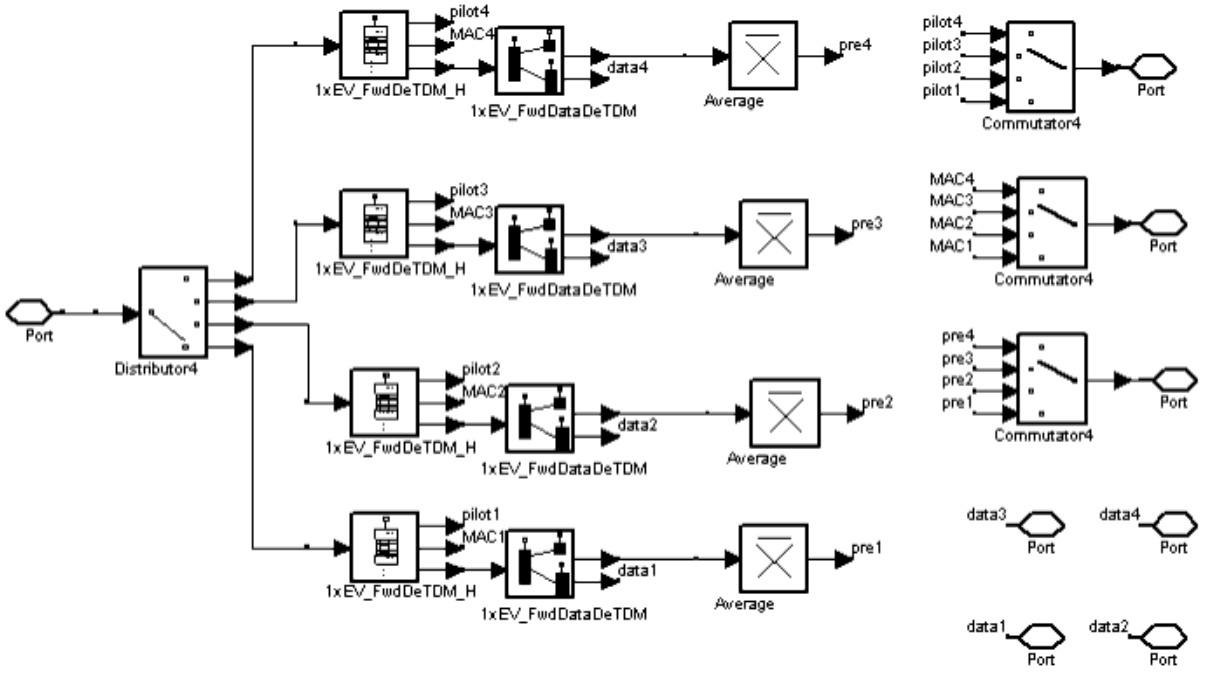
Pin	Name	Description	Signal Type
1	Input	time-division-multiplexed data	complex

Pin Outputs

Pin	Name	Description	Signal Type
2	Data1	data from the first packet in the forward traffic channel or control channel	complex
3	Data2	data from the second packet in the forward traffic channel or control channel	complex
4	Data3	data from the third packet in the forward traffic channel or control channel	complex
5	Data4	data from the fourth packet in the forward traffic channel or control channel	complex
6	Preamb	preamble	real
7	MAC	MAC data	complex
8	Pilot	pilot	real

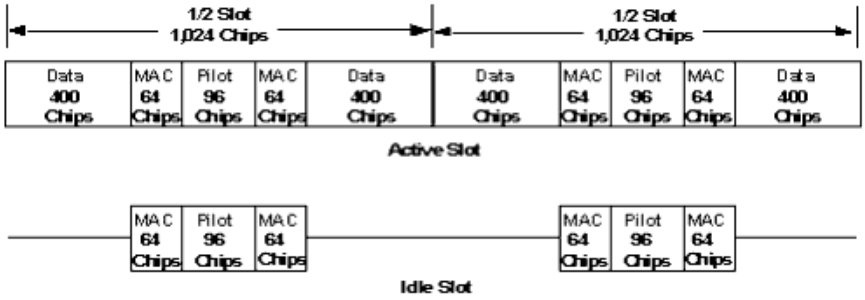
Notes/Equations

1. This subnetwork is used to time-division-demultiplex the channels of forward link for different data rate.
2. This subnetwork can support demultiplexing up to 4 packets at the same time. If 4 instances of this subnetwork are used, 16 packets, for up to 16 users, can be demultiplexed. The data rate of each packet can be set separately by setting DataRate1-DataRate4. The schematic for 1xEV_FwdDeTDM is shown in the following figure.



1xEV_FwdDeTDM Subnetwork

3. The forward link consists of slots of length 2048 chips (1.66 ms). Groups of 16 slots align to the PN rolls of the zero-offset PN sequences and align to system time on even-second ticks.
4. Within each slot, the Pilot, MAC, and Traffic or Control Channels are time-division multiplexed as shown in the following figure.



Forward Link Slot Structure

5. Forward traffic channel and control channel physical layer packets can be transmitted in 1 to 16 slots according to the following table. When more than one slot is allocated, the transmit slots use 4-slot interlacing, that is, the transmit slots of a packet are separated by three intervening slots, and slots of other packets are transmitted in the slots between those transmit slots.

Forward Traffic Channel and Control Channel Modulation Parameters

Data Rate (kbps)	Physical Layer Packet Values							
	Slots	Bits	Code Rate	Modulation Type	TDM Chips			
					Preamble	Pilot	MAC	Data
38.4	16	1,024	1/5	QPSK	1,024	3,072	4,096	24,576
76.8	8	1,024	1/5	QPSK	512	1,536	2,048	12,288
153.6	4	1,024	1/5	QPSK	256	768	1,024	6,144
307.2	2	1,024	1/5	QPSK	128	384	512	3,072
614.4	1	1,024	1/3	QPSK	64	192	256	1536
307.2	4	2,048	1/3	QPSK	128	768	1024	6,272
614.4	2	2,048	1/3	QPSK	64	384	512	3,136
1,228.8	1	2,048	1/3	QPSK	64	192	256	1,536
921.6	2	3,072	1/3	8PSK	64	384	512	3,136
1,843.2	1	3,072	1/3	8PSK	64	192	256	1,536
1,228.8	2	4,096	1/3	16QAM	64	384	512	3,136
2,457.6	1	4,096	1/3	16QAM	64	192	256	1,536

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_FwdTDM

Description: Time division multiplex for forward link
Library: 1xEV, Modems
Class: SDF1xEV_FwdTDM

Parameters

Name	Description	Default	Unit	Type	Range
SlotState	state of each slot: 0 for idle, 1 for active	1 0 0 0		int array	0:1
DataRate1	data rate of the first packet in the forward traffic channel: RateA01, RateA02, RateA03, RateA04, RateA05, RateA06, RateA07, RateA08, RateA09, RateA10, RateA11, RateA12	RateA01		enum	†
DataRate2	data rate of the second packet in the forward traffic channel: RateB01, RateB02, RateB03, RateB04, RateB05, RateB06, RateB07, RateB08, RateB09, RateB10, RateB11, RateB12	RateB01		enum	†
DataRate3	data rate of the third packet in the forward traffic channel: RateC01, RateC02, RateC03, RateC04, RateC05, RateC06, RateC07, RateC08, RateC09, RateC10, RateC11, RateC12	RateC01		enum	†
DataRate4	data rate of the fourth packet in the forward traffic channel: RateD01, RateD02, RateD03, RateD04, RateD05, RateD06, RateD07, RateD08, RateD09, RateD10, RateD11, RateD12	RateD01		enum	†

† DataRate1 to DataRate4 is the same parameter for different packets, the label in schematic for each rate is as follows: R38.4kbps 16 slot, R76.8kbps 8 slot, R153.6kbps 4 slot, R307.2kbps 2 slot, R614.4kbps 1 slot, R307.2kbps 4 slot, R614.4kbps 2 slot, R1228.8kbps 1 slot, R921.6kbps 2 slot, R1843.2kbps 1 slot, R1228.8kbps 2 slot, R2457.6kbps 1 slot.

Pin Inputs

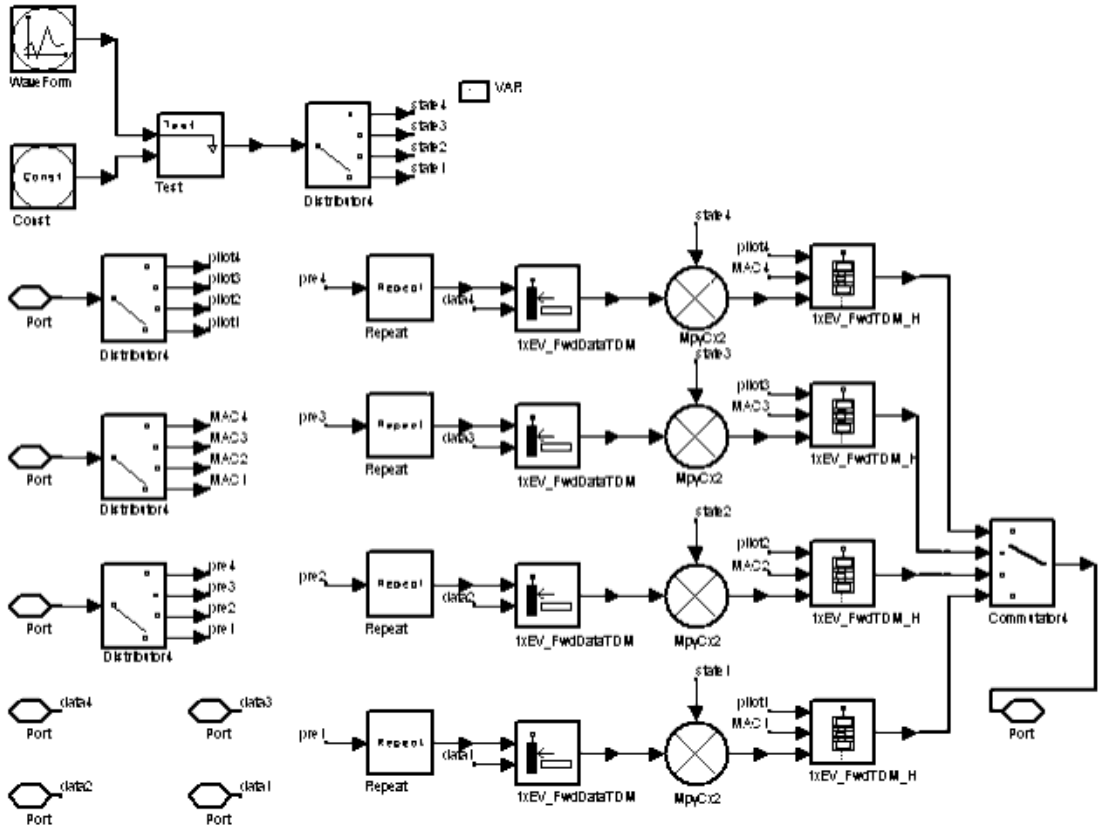
Pin	Name	Description	Signal Type
1	Data1	data from the first packet in the forward traffic channel or control channel	complex
2	Data2	data from the second packet in the forward traffic channel or control channel	complex
3	Data3	data from the third packet in the forward traffic channel or control channel	complex
4	Data4	data from the fourth packet in the forward traffic channel or control channel	complex
5	Preamb	preamble	real
6	MAC	MAC data	complex
7	Pilot	pilot data	real

Pin Outputs

Pin	Name	Description	Signal Type
8	Output	time-division-multiplexed data	complex

Notes/Equations

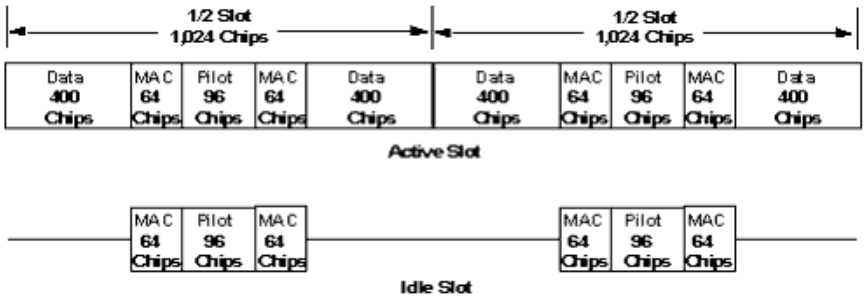
1. This subnetwork is used to time-division-multiplex forward link channels. The schematic for this subnetwork is shown in the following figure.



1xEV_FwdTDM Schematic

2. Slots can be set active or idle in the SlotState parameter. When set to active, traffic channel data will be transmitted with pilot and MAC data; when set to idle, only pilot and MAC data will be transmitted.
3. This subnetwork supports transmitting up to 4 packets at the same time. If 4 instances of this subnetwork are used, 16 packets, for up to 16 users, can be transmitted together. The data rate of each packet can be set separately by setting DataRate parameters. Packets will be transmitted in 4-slot interlacing.

   (This subnetwork does not support changing data rate according to channel condition.)
4. Preamble and traffic or control channel data are combined as data before TDM. 1xEV_FwdDataTDM is used to time-division-multiplex the preamble and data from forward traffic channel or forward control channel according to the data rate. Data then will be multiplexed with pilot, MAC to form the forward link signal by 1xEV_FwdTDM_H.
5. The forward link consists of slots of length 2048 chips (1.66 ms). Groups of 16 slots are aligned to the PN rolls of the zero-offset PN sequences and align to system time on even-second ticks.
6. Within each slot, the pilot, MAC, and traffic or control channels are time-division multiplexed as shown in the following figure. All time-division-multiplexed channels are transmitted at the maximum power of the sector.



Forward Link Slot Structure

7. Forward traffic and control channel physical layer packets can be transmitted in 1 to 16 slots (see the table below). When more than one slot is allocated, the transmit slots uses 4-slot interlacing; that is, the transmit slots of a packet are separated by three intervening slots and slots of other packets are transmitted in the slots between those transmit slots.

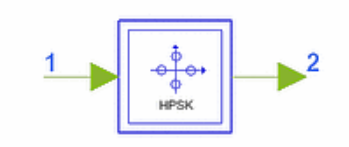
Modulation Parameters for Forward Traffic and Control Channels

Data Rate (kbps)	Physical Layer Packet Values							
	Slots	Bits	Code Rate	Modulation Type	TDM Chips			
					Preamble	Pilot	MAC	Data
38.4	16	1,024	1/5	QPSK	1,024	3,072	4,096	24,576
76.8	8	1,024	1/5	QPSK	512	1,536	2,048	12,288
153.6	4	1,024	1/5	QPSK	256	768	1,024	6,144
307.2	2	1,024	1/5	QPSK	128	384	512	3,072
614.4	1	1,024	1/3	QPSK	64,	192	256	1536
307.2	4	2,048	1/3	QPSK	128	768	1024	6,272
614.4	2	2,048	1/3	QPSK	64	384	512	3,136
1,228.8	1	2,048	1/3	QPSK	64	192	256	1,536
921.6	2	3,072	1/3	8PSK	64	384	512	3,136
1,843.2	1	3,072	1/3	8PSK	64	192	256	1,536
1,228.8	2	4,096	1/3	16QAM	64	384	512	3,136
2,457.6	1	4,096	1/3	16QAM	64	192	256	1,536

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_HPSK



Description: Quadrature spreading for 1xEV reverse link
Library: 1xEV, Modems
Class: SDF1xEV_HPSK

Parameters

Name	Description	Default	Unit	Type	Range
ChannelType	type of channel: Access Channel, Reverse Traffic Channel	Reverse Traffic Channel		enum	
ATI_low	lower 16 bits of access terminal identifier	0		int	[0:65535]
ATI_high	higher 16 bits access terminal identifier	0		int	[0:65535]
AccessCycleNumber	access cycle number	0		int	[0:255]
ColorCode	color code	0		int	[0:255]
SectorID	sector ID	0		int	[0:16777215]
TransDelay	transmit delay	0		int	[0, ∞)
Q_Phase	sign of sine: Sine, Minus Sine	Sine		enum	

Pin Inputs

Pin	Name	Description	Signal Type
1	Input	input data	complex

Pin Outputs

Pin	Name	Description	Signal Type
2	Output	output data	complex

Notes/Equations

1. This subnetwork is used to implement HPSK for 1xEV reverse link.

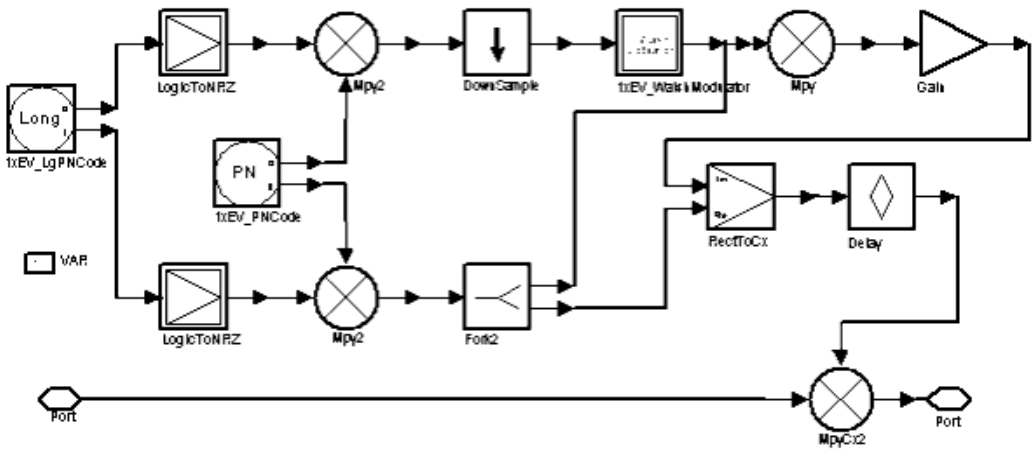
   The schematic for this subnetwork is shown in the figure below. The I-Channel data and Q-Channel data are complex multiplied by a complex spreading sequence before baseband filtering.

   The in-phase spreading sequence is formed by a modulo-2 addition of the I-channel PN sequence and the I long code sequence.

   The quadrature-phase spreading sequence is formed by a modulo-2 addition of: a W12 Walsh sequence, the modulo-2 addition of the I-channel PN sequence and the I long code sequence, and the modulo-2 addition of the Q-channel PN sequence and the Q long code sequence decimated by 2.
2. The spectrum can be centered to ωc or $-\omega_c$ when baseband signal modulating the carrier. While $-\omega_c$ is generally used, the spectrum must be centered to ωc according to 1xEV standard [1].

   Q_Phase is used to adjust the phase of Q modulated signal. If

- Q_Phase = Sine, the spectrum is centered to ωc
- Q_Phase = Minus Sine, the spectrum is centered to $-\omega_c$.

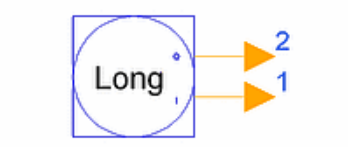


1xEV_HPSK Schematic

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_LgPNCode



Description: Long code generator
Library: 1xEV, Modems
Class: SDF1xEV_LgPNCode

Parameters

Name	Description	Default	Unit	Type	Range
ChannelType	type of channel: Access Channel, Reverse Traffic Channel	Reverse Traffic Channel		enum	
ATI_low	lower 16 bits of access terminal identifier	0		int	[0:65535]
ATI_high	higher 16 bits access terminal identifier	0		int	[0:65535]
AccessCycleNumber	access cycle number	0		int	[0:255]
ColorCode	color code	0		int	[0:255]
SectorID	sector ID	0		int	[0:16777215]

Pin Outputs

Pin	Name	Description	Signal Type
1	U_I	long PN code I	int
2	U_Q	long PN code Q	int

Notes/Equations

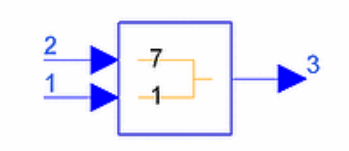
1. This model is used to generate long PN code for 1xEV reverse link.

   Each firing, 1 U_I token and 1 U_Q token are produced.

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_MAC_TDM



Description: Time-division-multiplexer for MAC Channel RPC bits and DRCLock symbols
Library: 1xEV, Modems
Class: SDF1xEV_MAC_TDM

Parameters

Name	Description	Default	Unit	Type	Range
Version	version of cdma2000 High Rate Packet Data Air Interface Specification: C_P9010, C_S0024	C_P9010		enum	
DRC_LockPeriod	the time interval in units of slots between transmission of two consecutive DRCLock bit: _8_Slots, _16_Slots	_8_Slots		enum	

Pin Inputs

Pin	Name	Description	Signal Type
1	DRC	DRCLock symbols	real
2	RPC	RPC bits	real

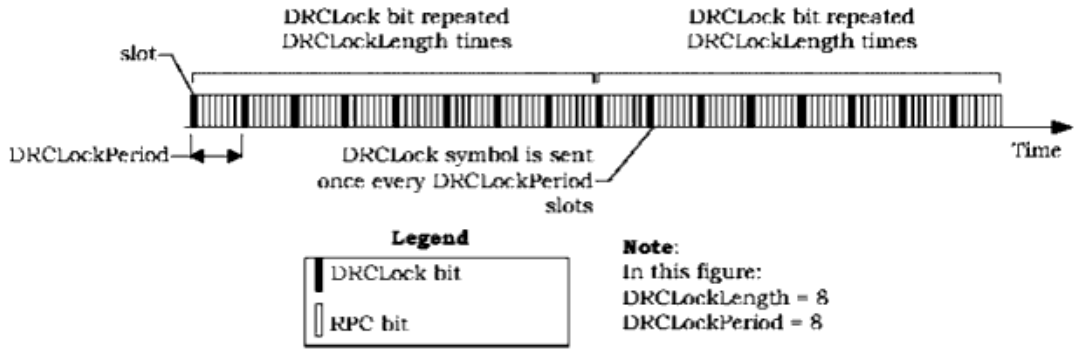
Pin Outputs

Pin	Name	Description	Signal Type
3	Output	time-division-multiplexed RPC and DRCLock	real

Notes/Equations

1. This model time-division-multiplexes RPC bits and DRCLock symbols for MAC channel. If Version is set to _C_P9010 (_ DRCLock channel is not supported) data is copied from the *RPC* input to the *Output*; if Version is set to _C_S0024_, data from DRCLock and RPC channels are time-division-multiplexed.

   Each firing, when Version is set to _C_P9010_, one Output token is produced when one DRC token and one RPC token are consumed; when Version is set to _C_S0024_, DRC_LockPeriod Output tokens are produced when one DRC token and DRC_LockPeriod-1 RPC tokens are consumed. (Note that, when Version is set to _C_P9010_, DRC tokens are not used.)
2. The RPC and DRCLock channels are time-division multiplexed and transmitted on the same MAC Channel. The RPC channel is transmitted in DRC_LockPeriod-1 slots out of every DRC_LockPeriod slots, where DRC_LockPeriod is given as public data by the Forward Traffic Channel MAC Protocol. The RPC data rate is 600 × (1 - 1/DRC_LockPeriod) bps.
3. The DRCLock channel is transmitted in one out of every DRC_LockPeriod slots. Each DRCLock bit is repeated and transmitted in DRCLockLength slots, where DRCLockLength is given as public data by the Forward Traffic Channel MAC Protocol. The DRCLock data rate is 600/(DRCLockLength × DRC_LockPeriod) bps.
4. An example for transmission of DRCLock bits with DRCLockLength = 8 and DRC_LockPeriod = 8 is illustrated in the following figure.



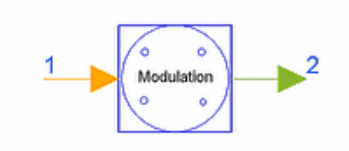
DRCLock Puncturing Example

5. Data from DRCLock channel and data from RPC are multiplexed as shown in the figure. DRCLock symbols should be repeated before input to this model.

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification*, Version 2.1, August 23, 2001.

1xEV_Modulator



Description: Modulator to generate QPSK, 8-PSK, 16-QAM modulation symbols depending on data rate
Library: 1xEV, Modems
Class: SDF1xEV_Modulator

Parameters

Name	Description	Default	Unit	Type	Range
DataRate	data rate of the forward traffic channel: R38.4kbps 16 slot, R76.8kbps 8 slot, R153.6kbps 4 slot, R307.2kbps 2 slot, R614.4kbps 1 slot, R307.2kbps 4 slot, R614.4kbps 2 slot, R1228.8kbps 1 slot, R921.6kbps 2 slot, R1843.2kbps 1 slot, R1228.8kbps 2 slot, R2457.6kbps 1 slot	R38.4kbps 16 slot		enum	

Pin Inputs

Pin	Name	Description	Signal Type
1	Input	input data	int

Pin Outputs

Pin	Name	Description	Signal Type
2	Output	output modulation symbols	complex

Notes/Equations

1. This model is used to generate QPSK, 8PSK, 16QAM modulation symbols for 1xEV/DO forward link depending on the data rate.

   The table below shows the modulation parameter for forward traffic channel and control channel. For each data rate, the modulation type is: QPSK, 8PSK, or 16QAM.

   Each firing, if the modulation type is QPSK, one output token is produced when two input tokens are consumed; if the modulation type is 8PSK, one output token is produced when three input tokens are consumed. If the modulation type is 16QAM, one output token is produced when four input tokens are consumed.

Modulation Parameters for Forward Traffic and Control Channels

Data Rate (kbps)	Number of Values per Physical Layer Packet		
	Slot	Bits	Modulation Type
38.4	16	1,024	QPSK
76.8	8	1,024	QPSK
153.6	4	1,024	QPSK
307.2	2	1,024	QPSK
614.4	1	1,024	QPSK
307.2	4	2,048	QPSK
614.4	2	2,048	QPSK
1,228.8	1	2,048	QPSK
921.6	2	3,072	8PSK
1,843.2	1	3,072	8PSK
1,228.8	2	4,096	16QAM
2,457.6	1	4,096	16QAM

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_PhaseEqualizer

Description: Filter to provide phase equalization
Library: 1xEV, Modems
Class: SDF1xEV_PhaseEqualizer

Parameters

Name	Description	Default	Unit	Type	Range
Type	filter used at transmitter side or receiver side: Transmitter, Receiver	Transmitter		enum	
SampPerChip	samples per chip: Rate4, Rate5, Rate6, Rate8	Rate4		enum	

Pin Inputs

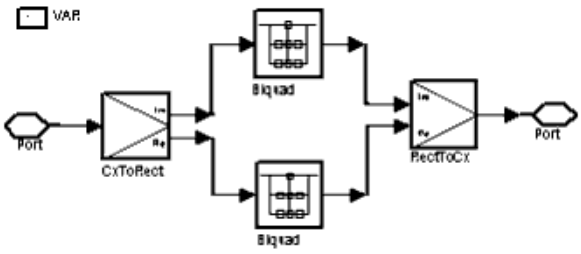
Pin	Name	Description	Signal Type
1	Input	input signal from baseband filter	complex

Pin Outputs

Pin	Name	Description	Signal Type
2	Output	output signal of phase equalizing filter	complex

Notes/Equations

1. This subnetwork provides phase equalization for the transmit signal path. The schematic for this subnetwork is shown in the following figure.



1xEV_PhaseEqualizer Schematic

1. Each firing, one Output token is produced when one Input token is consumed.
2. The equalizing filter provides the equivalent baseband transfer function

$$H(\omega) = K\frac{\omega^2 + j\alpha\omega\omega_0 - \omega_0^2}{\omega^2 - j\alpha\omega\omega_0 - \omega_0^2}$$

where K is an arbitrary gain, j equals $\sqrt{-1}$, $\alpha = 1.36$, $\omega 0 = 2\pi \times 3.15 \times 10^5$, and ω is the radian

frequency.

The equalizing filter implementation is equivalent to individually applying baseband filters with this transfer function to the baseband I and Q waveforms.

3. According to this analog filter, an IIR allpass filter design has the following transfer function:

$$H(z) = \frac{1 + b_1 z + b_2 z^2}{z^2 + b_1 z + b_2}$$

The table below lists the recommended *b* 1 and *b* 2 coefficients for the respective oversampling rates according to [2].

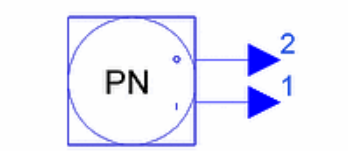
Recommended Coefficients

Oversampling Rate	b0	b1	b2
4	1	-1.45514	0.57832
5	1	-1.56195	0.64526
6	1	-1.63412	0.69414
8	1	-1.72513	0.76047

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.
2. Analog Devices, "Data Sheet 11-8-2000, AD6623," REV.PrB.

1xEV_PNCode



Description: Short PN code generator
Library: 1xEV, Modems
Class: SDF1xEV_PNCode

Parameters

Name	Description	Default	Unit	Type	Range
PN_Offset	access terminal PN code offset	0		int	[0:511]
Link	type of link: Forward link, Reverse link	Forward link		enum	

Pin Outputs

Pin	Name	Description	Signal Type
1	PN_I	PN code I	real
2	PN_Q	PN code Q	real

Notes/Equations

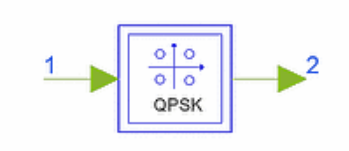
1. This model is used to generate short PN code for reverse and forward links.

   Each firing, one PN_I token and one PN_Q token are produced.

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_QPSK



Description: Quadrature spreading for 1xEV forward link
Library: 1xEV, Modems
Class: SDF1xEV_QPSK

Parameters

Name	Description	Default	Unit	Type	Range
PN_Offset	offset of short PN code	0		int	[0:511]
TransDelay	transmit delay	0		int	[0, ∞)
Q_Phase	sign of sine: Sine, Minus Sine	Sine		enum	

Pin Inputs

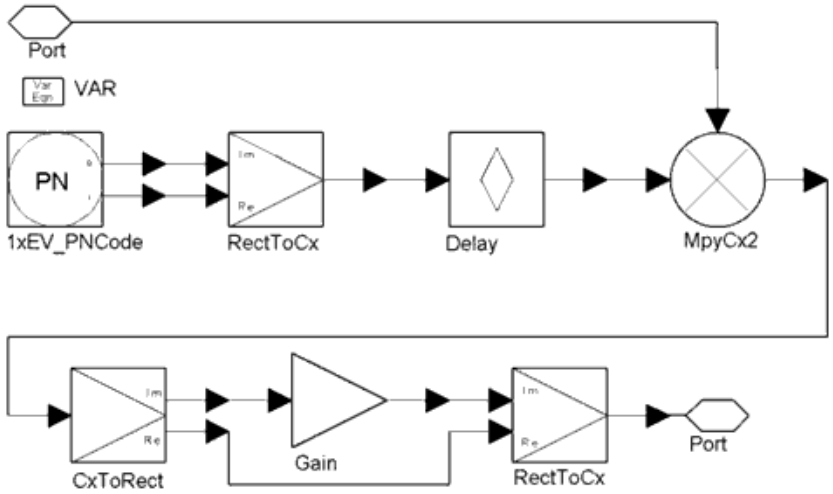
Pin	Name	Description	Signal Type
1	D_in	input data	complex

Pin Outputs

Pin	Name	Description	Signal Type
2	D_out	output data	complex

Notes/Equations

1. This subnetwork is used to implement QPSK modulation for 1xEV forward link. Input data is spread by PN codes of the I and Q phases. The schematic for this subnetwork is shown in the figure below.
2. The spectrum can be centered to ωc or -ωc when baseband signal modulating the carrier. While -ωc is generally used, the spectrum must be centered to ωc according to 1xEV standard [1]. So, a parameter is added to adjust the phase of Q modulated signal. If
   - Q_Phase = Sine, the spectrum is centered to ωc
   - Q_Phase = Minus Sine, the spectrum is centered to -ωc.

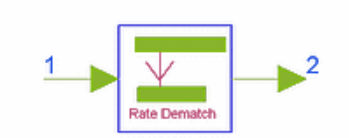


1xEV_QPSK Schematic

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_RateDematch



Description: Rate dematching for forward link
Library: 1xEV, Modems
Class: SDF1xEV_RateDematch

Parameters

Name	Description	Default	Unit	Type	Range
DataRate	data rate of the forward traffic channel: R38.4kbps 16 slot, R76.8kbps 8 slot, R153.6kbps 4 slot, R307.2kbps 2 slot, R614.4kbps 1 slot, R307.2kbps 4 slot, R614.4kbps 2 slot, R1228.8kbps 1 slot, R921.6kbps 2 slot, R1843.2kbps 1 slot, R1228.8kbps 2 slot, R2457.6kbps 1 slot	R38.4kbps 16 slot		enum	

Pin Inputs

Pin	Name	Description	Signal Type
1	Data	data from QPSK/8PSK/16-QAM modulator	complex

Pin Outputs

Pin	Name	Description	Signal Type
2	Output	rate matched data	complex

Notes/Equations

1. This model rate-dematches the forward link. Each firing, M tokens are produced when N tokens are consumed, where N and M modulation symbols are provided according to the following table.

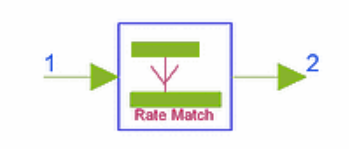
Sequence Repetition and Symbol Puncturing Parameters

Data Rate (kbps)	Values per Physical Layer Packet						Approximate Coding	
	Number of Slots	Number of Bits	Number of Modulation Symbols Provided (M)	Number of Modulation Symbols Needed (N)	Number of Full Sequence Transmissions	Number of Modulation Symbols in Last Partial Transmission	Code Rate	Repetition Factor
38.4	16	1,024	2,560	24,576	9	1,536	1/5	9.6
76.8	8	1,024	2,560	12,288	4	2,048	1/5	4.8
153.6	4	1,024	2,560	6,144	2	1,024	1/5	2.4
307.2	2	1,024	2,560	3,072	1	512	1/5	1.2
614.4	1	1,024	1,536	1,536	1	0	1/3	1
307.2	4	2,048	3,072	6,272	2	128	1/3	2.04
614.4	2	2,048	3,072	3,136	1	64	1/3	1.02
1,228.8	1	2,048	3,072	1,536	0	1,536	1/3	1
921.6	2	3,072	3,072	3,136	1	64	1/3	1.02
1,843.2	1	3,072	3,072	1,536	0	1,536	1/3	1
1,228.8	2	4,096	3,072	3,136	1	64	1/3	1.02
2,457.6	1	4,096	3,072	1,536	0	1,536	1/3	1

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_RateMatch



Description: Sequence repetition and symbol puncturing for forward link
Library: 1xEV, Modems
Class: SDF1xEV_RateMatch

Parameters

Name	Description	Default	Unit	Type	Range
DataRate	data rate of the forward traffic channel: R38.4kbps 16 slot, R76.8kbps 8 slot, R153.6kbps 4 slot, R307.2kbps 2 slot, R614.4kbps 1 slot, R307.2kbps 4 slot, R614.4kbps 2 slot, R1228.8kbps 1 slot, R921.6kbps 2 slot, R1843.2kbps 1 slot, R1228.8kbps 2 slot, R2457.6kbps 1 slot	R38.4kbps 16 slot		enum	

Pin Inputs

Pin	Name	Description	Signal Type
1	Data	data from QPSK/8PSK/16-QAM modulator	complex

Pin Outputs

Pin	Name	Description	Signal Type
2	Output	rate matched data	complex

Notes/Equations

1. This component is used to match the rate of forward link. It includes sequence repetition and symbol puncturing according to the following table. Each firing, M tokens are produced when N tokens are consumed.

Sequence Repetition and Symbol Puncturing Parameters

Data Rate (kbps)	Values per Physical Layer Packet						Approximate Coding	
	Number of Slots	Number of Bits	Number of Modulation Symbols Provided (N)	Number of Modulation Symbols Needed (M)	Number of Full Sequence Transmissions	Number of Modulation Symbols in Last Partial Trans mission	Code Rate	Repetition Factor
38.4	16	1,024	2,560	24,576	9	1,536	1/5	9.6
76.8	8	1,024	2,560	12,288	4	2,048	1/5	4.8
153.6	4	1,024	2,560	6,144	2	1,024	1/5	2.4
307.2	2	1,024	2,560	3,072	1	512	1/5	1.2
614.4	1	1,024	1,536	1,536	1	0	1/3	1
307.2	4	2,048	3,072	6,272	2	128	1/3	2.04
614.4	2	2,048	3,072	3,136	1	64	1/3	1.02
1,228.8	1	2,048	3,072	1,536	0	1,536	1/3	1
921.6	2	3,072	3,072	3,136	1	64	1/3	1.02
1,843.2	1	3,072	3,072	1,536	0	1,536	1/3	1
1,228.8	2	4,096	3,072	3,136	1	64	1/3	1.02
2,457.6	1	4,096	3,072	1,536	0	1,536	1/3	1

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_RevPowerAdjust

Description: Power adjuster for access terminal channels
Library: 1xEV, Modems
Class: SDF1xEV_RevPowerAdjust

Parameters

Name	Description	Default	Unit	Type	Range
TrafficAdjustStep	power adjust step: Step0dB, Step0_5dB, Step1dB	Step0dB		enum	
BlockSize	number of particles in a block	2048		int	[1, ∞)
IgnoreNum	number of initially ignored firings	1		int	[0, ∞)

Pin Inputs

Pin	Name	Description	Signal Type
1	D_in	input data	complex
2	PCBit	power control bits	int

Pin Outputs

Pin	Name	Description	Signal Type
3	D_out	output data	complex

Notes/Equations

1. This model is used to adjust the power of access terminal.

   Each firing, BlockSize D_out tokens are produced when BlockSize D_in and one PCBit token are consumed.

   If PCBit is 0, the access terminal will increase power at a TrafficAdjustStep value; otherwise, the access terminal will decrease power at a TrafficAdjustStep value. The total closed-loop adjustment range is ±80 dB around its open-loop estimate.

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_ScrambleCode

Description: Scrambling sequence generator
Library: 1xEV, Modems
Class: SDF1xEV_ScrambleCode

Parameters

Name	Description	Default	Unit	Type	Range
MAC_Index	preamble MACIndex	2		int	2:3:[5:63]
DataRate	data rate of the forward traffic channel: R38.4kbps 16 slot, R76.8kbps 8 slot, R153.6kbps 4 slot, R307.2kbps 2 slot, R614.4kbps 1 slot, R307.2kbps 4 slot, R614.4kbps 2 slot, R1228.8kbps 1 slot, R921.6kbps 2 slot, R1843.2kbps 1 slot, R1228.8kbps 2 slot, R2457.6kbps 1 slot	R38.4kbps 16 slot		enum	

Pin Outputs

Pin	Name	Description	Signal Type
1	output	output of shift register	int

Notes/Equations

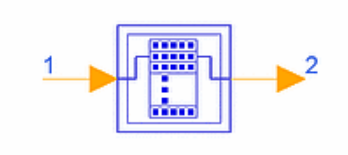
1. This model is used to generate scrambling code for forward traffic channel.

   Each firing, one output token is produced.

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_SimplexEncoder



Description: 1xEV simplex encoder
Library: 1xEV, Modems
Class: SDF1xEV_SimplexEncoder

Pin Inputs

Pin	Name	Description	Signal Type
1	In	input data	int

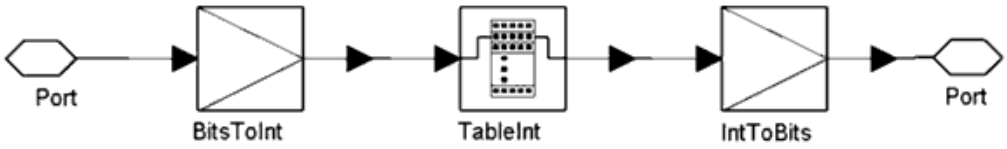
Pin Outputs

Pin	Name	Description	Signal Type
2	Out	output data	int

Notes/Equations

1. This subnetwork is used to encode reverse rate indicator (RRI) channel. The schematic for this subnetwork is shown in the figure below.

   Each firing, three input tokens are consumed and seven output tokens are produced.



1xEV_SimplexEncoder Schematic

2. RRI channel symbol and encoder assignments are listed in the table below.

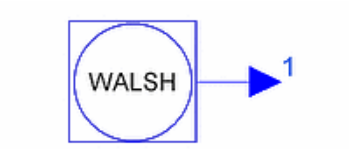
RRI Symbol and Simplex Encoder Assignments

Data Rate (kbps)	RRI Symbol	RRI Codeword
0	000	0000000
9.6	001	1010101
19.2	010	0110011
38.4	011	1100110
76.8	100	0001111
153.6	101	1011010
Reserved	110	0111100
Reserved	111	1101001

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_WalshCode



Description: Walsh code generator
Library: 1xEV, Modems
Class: SDF1xEV_WalshCode

Parameters

Name	Description	Default	Symbol	Unit	Type	Range
WalshLength	length of Walsh code	64	N		int	2^n, n=1,...,11
WalshCodeIndex	index of Walsh code	0			int	[0:2^n- 1], n = 1,...,11

Pin Outputs

Pin	Name	Description	Signal Type
1	Walsh	Walsh code	real

Notes/Equations

1. This model is used to generate variable length Walsh code symbols.

   Each firing, N tokens are produced, where N is the Walsh code length.

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification*, Version 2.1, August 23, 2001.

1xEV_WalshCover

Description: FHT is performed to realize Walsh cover and chip level summer
Library: 1xEV, Modems
Class: SDF1xEV_WalshCover

Parameters

Name	Description	Default	Symbol	Unit	Type	Range
WalshLength	the length of Walsh code used for spreading	16	N		int	2^n, n=1,...,11

Pin Inputs

Pin	Name	Description	Signal Type
1	D_in	input data	complex

Pin Outputs

Pin	Name	Description	Signal Type
2	D_out	output data	complex

Notes/Equations

1. This component is used to perform Walsh cover and chip level summer using FHT.

   Each firing, N tokens of D_out are produced when N tokens of D_in are consumed.

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_WalshModulator

Description: Walsh code modulator
Library: 1xEV, Modems
Class: SDF1xEV_WalshModulator

Parameters

Name	Description	Default	Symbol	Unit	Type	Range
WalshLength	length of Walsh code	64	N		int	2^n, n=1,...,11
WalshCodeIndex	index of Walsh code	0			int	[0:2^n- 1], n=1,...,11

Pin Inputs

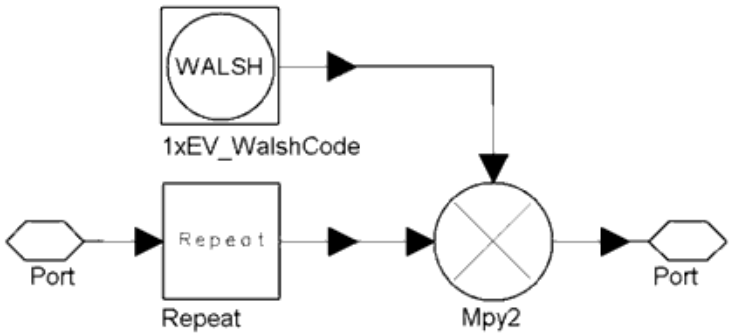
Pin	Name	Description	Signal Type
1	D_in	input data	real

Pin Outputs

Pin	Name	Description	Signal Type
2	D_out	output data	real

Notes/Equations

1. This subnetwork is used to spread input data to WalshLength chips with the Walsh Code sequence of corresponding length and index.
2. The schematic for this subnetwork is shown in the following figure.



1xEV_WalshModulator Schematic

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

Power Amplifier Design Examples

Introduction

The 1xEV power amplifier workspace (1xEV_PA_Test_wrk) provides design and verification solutions for 1xEV network and terminal access. Example designs included for this workspace are described in the following sections.

- DSN_1xEV_FwdPower for forward link power measurement
- DSN_1xEV_FwdRho for forward link Rho measurement
- DSN_1xEV_RevRho for reverse link Rho measurement
- DSN_1xEV_FwdCDP for code domain power measurement

Forward Link Code Domain Power Measurement

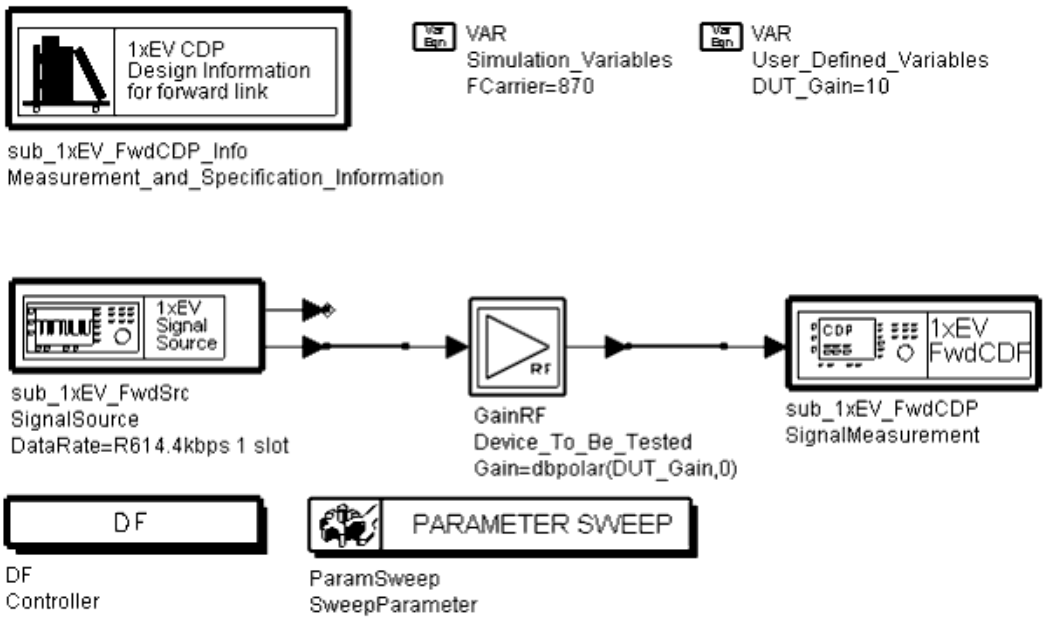
- DSN_1xEV_FwdCDP

Description

This design is used to measure forward link code domain power in compliance with 3GPP2 C.P9011 specification [2].

Code-domain power *p* (*i*) is defined as the fractional energy of the signal under test that correlates with the reference signal for the *i* th code channel.

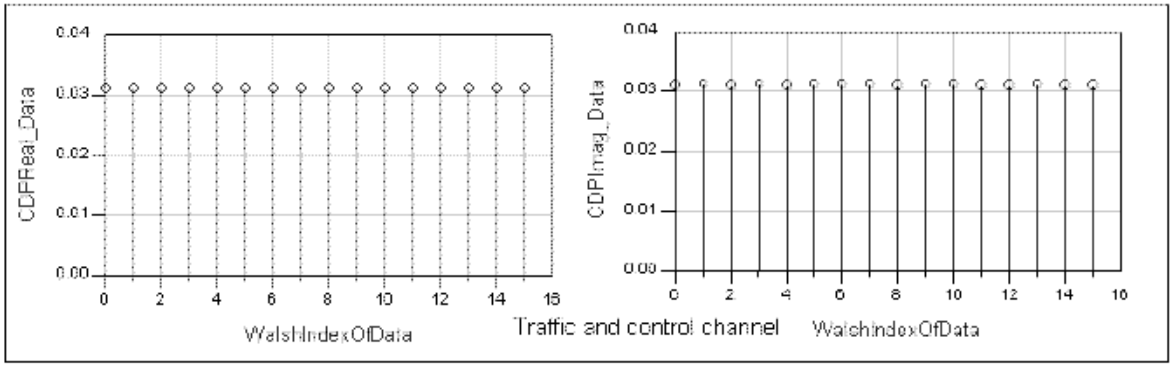
The top-level schematic for this design is shown in the following figure. The Measurement_and_Specification_Information subnetwork contains measurement and relevant industrial specifications information. The SignalSource subnetwork generates RF band signal. The Device_To_Be_Tested subnetwork is the device to be tested-DUT_Gain is used for demonstration. The SignalMeasurement subnetwork implements the measurements. The CDP of the Forward Traffic and Control Channel and MAC Channel are measured with sub_1xEV_FwdCDP. Both for MAC Channel and the Forward Traffic and Control Channel, the sum of real and imaginary powers should be 1.0.



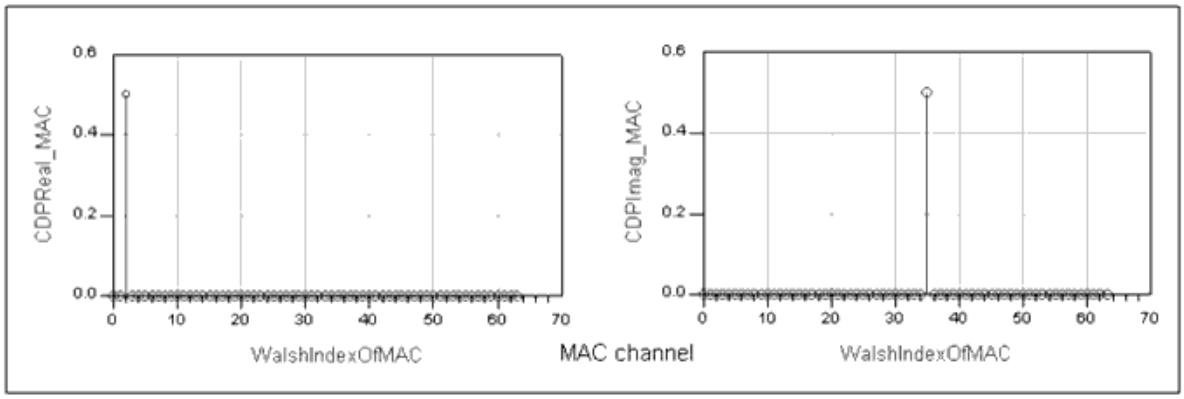
DSN_1xEV_FwdCDP Schematic

Simulation Results

Output variable CDPReal and CDPImag measurement results displayed in DSN_1xEV_FwdCDP.dds are shown in the following two figures.



Code Domain Power Measurements for Traffic and Control Channels



Code Domain Power Measurements for MAC Channel

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 1.5
- Simulation Time: approximately 70 seconds

References

1. 3GPP2 C.P9010, cdma2000 High Rate Packet Data Air Interface Specification, Ballot Resolution Version, September 12, 2000.
2. 3GPP2 C.P9011, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network, Dec.14, 2000.
3. 3GPP2 C.P9012, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Terminal, Dec.14, 2000.

Forward Link Power Measurement

- DSN_1xEV_FwdPower Design

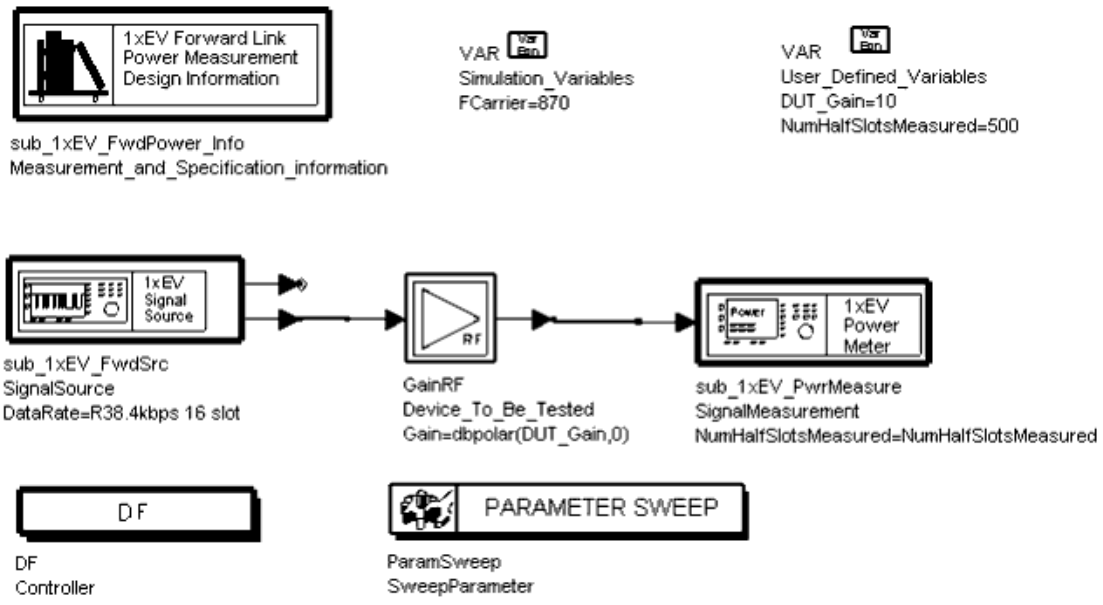
Description

This design is used to measure 1xEV forward link total power and pilot/MAC power.

When total power is measured, pilot, MAC, and traffic or control channels are time-division multiplexed; all time-division multiplexed channels are transmitted at equal power.

When pilot/MAC power is measured, pilot/MAC channels are transmitted in bursts of 224 chips every half slot.

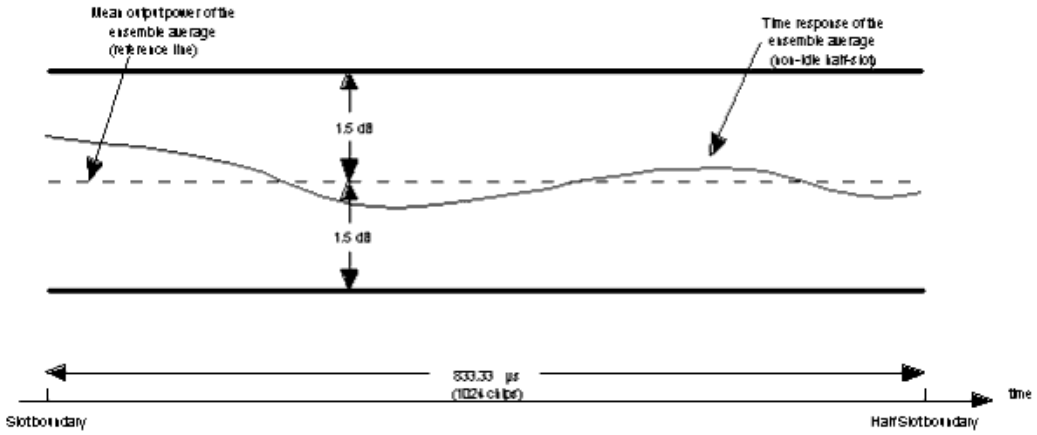
The top-level schematic for this design is shown in the following figure.



DSN_1xEV_FwdPower Schematic

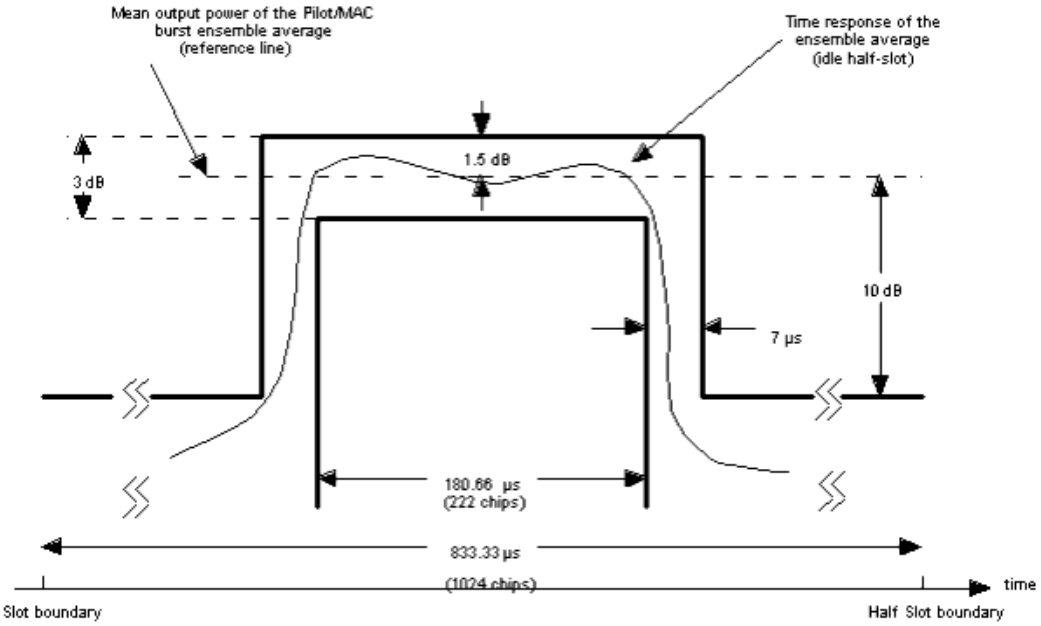
Minimum Standard

For non-idle half slots, the average time response average must be within the limits shown in the following figure.



Transmission Envelope Mask (Average Non-Idle Half Slot)

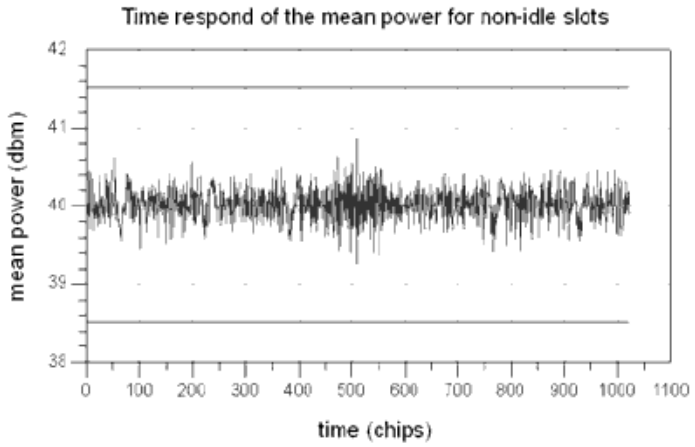
For idle half slots, the average time response must be within the limits shown in the following figure.



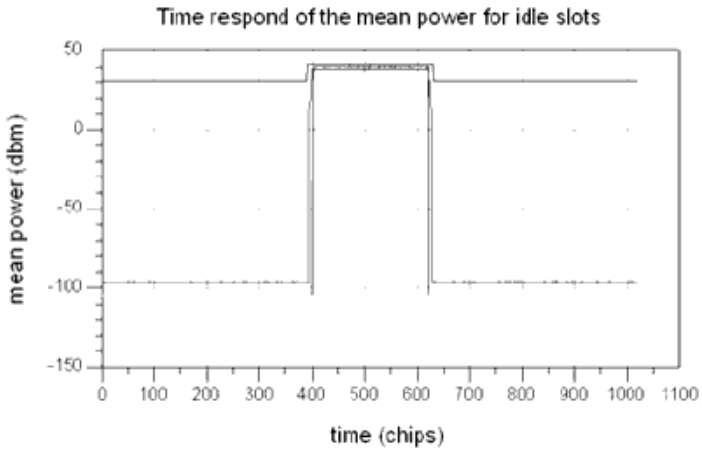
Transmission Envelope Mask (Average Idle Half Slot)

Simulation Results

Simulation results displayed in DSN_1xEV_FwdPower.dds are shown the following two figures. *Page Equations* shows equations that are used for threshold and variable definitions and calculations.



Time Response of Mean Power for Non-Idle Slots



Time Response of Mean Power for Idle Slots

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 1.5
- Simulation Time: approximately 12 minutes

References

1. 3GPP2 C.P9010, cdma2000 High Rate Packet Data Air Interface Specification, Ballot Resolution Version, September 12, 2000.
2. 3GPP2 C.P9011, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network, Dec. 14, 2000.

Forward Link Rho Measurement

- DSN_1xEV_FwdRho Design

Description

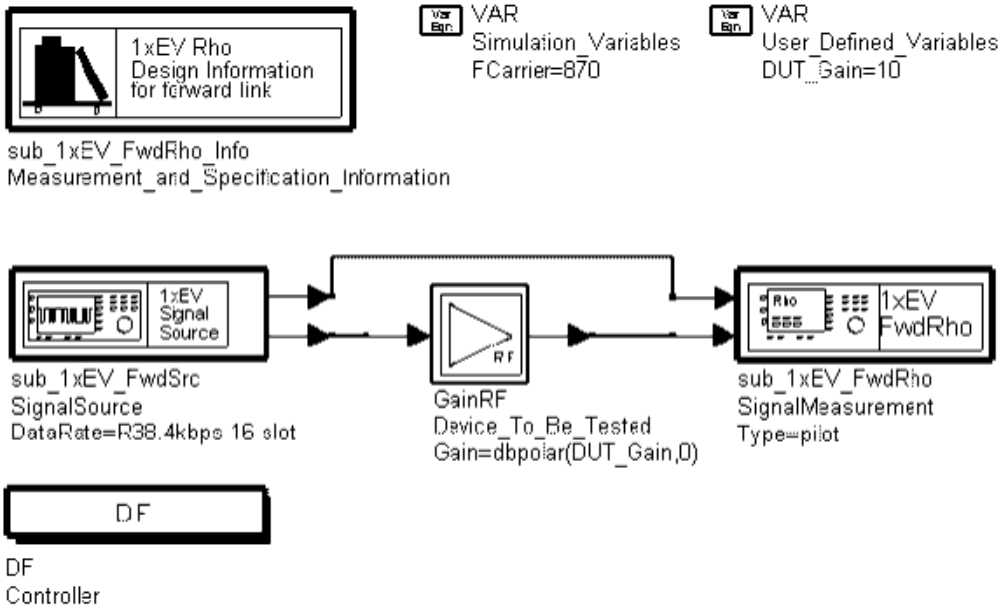
Modulation accuracy is the ability of the transmitter to generate the ideal signal. The cross-correlation Rho between the waveform representing the transmitted signal and the waveform representing the ideal signal is defined as a waveform quality factor.

The top-level schematic for this design is shown in the following figure. The Measurement_and_Specification_Information subnetwork contains measurement and relevant industrial specifications. The SignalSource subnetwork generates RF band signal for measurement. The Device_To_Be_Tested subnetwork is the device to be tested; DUT_Gain is used for demonstration. The SignalMeasurement subnetwork implements the Rho measurements.

The two data paths from the source to the measurement component are:

- one for the real transmitted signals which go through the device under test;
- one for the reference signals needed in the measurement.

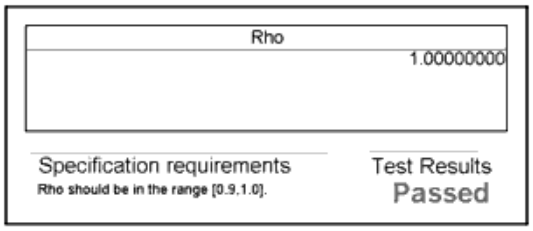
The output variable Rho is the parameter to be tested. According to the specification, rho should be larger than 0.9. Designers can set a threshold to satisfy their requirements in the DSN_1xEV_FwdRho.dds Equations window.



DSN_1xEV_FwdRho Schematic

Simulation Results

Simulation results displayed in DSN_1xEV_FwdRho.dds are shown in the following figure. Page Equations shows equations that are used for threshold and variable definitions and calculations.



Forward Link Rho Simulation Results

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 1.5
- Simulation Time: approximately 100 seconds

References

1. 3GPP2 C.P9010, cdma2000 High Rate Packet Data Air Interface Specification, Ballot Resolution Version, September 12, 2000.
2. 3GPP2 C.P9011, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network, Dec.14, 2000.
3. 3GPP2 C.P9012, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Terminal, Dec.14, 2000.

Reverse Link Rho Measurement

- DSN_1xEV_RevRho Design

Description

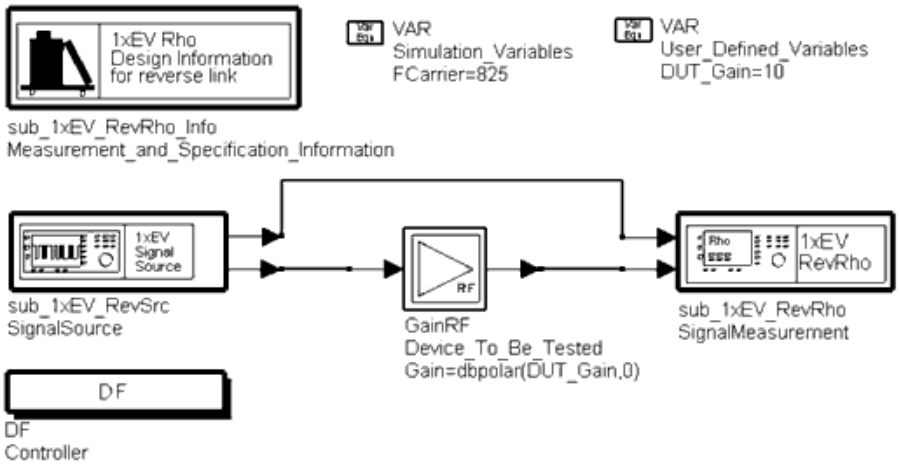
Modulation accuracy is the ability of the transmitter to generate the ideal signal. The cross-correlation Rho between the waveform representing the transmitted signal and the waveform representing the ideal signal is defined as a waveform quality factor.

The top-level schematic for this design is shown in the figure below. The Measurement_and_Specification_Information subnetwork contains measurement and relevant industrial specifications. The SignalSource subnetwork generates RF band signal for measurement. The Device_To_Be_Tested subnetwork is the device to be tested; DUT_Gain is used for demonstration. The SignalMeasurement subnetwork implements the Rho measurements.

The two data paths from the source to the measurement component are:

- one for the real transmitted signals which go through the device under test;
- one for the reference signals needed in the measurement.

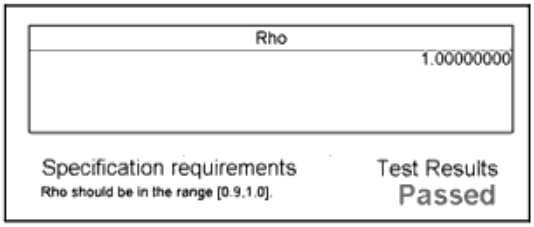
The output variable Rho is the parameter to be tested. According to the specification, Rho should be larger than 0.9. Designers can set a threshold to satisfy their own requirements in the window Equations of DSN_1xEV_RevRho.dds.



Schematic of DSN_1xEV_RevRho

Simulation Results

Simulation results displayed in DSN_1xEV_RevRho.dds are shown in the following figure. Page Equations is for the equations that are used for the threshold definitions and the variable definitions and calculations.



Reverse Link Rho Simulation Results

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 1.5
- Simulation Time: approximately 70 seconds

References

1. 3GPP2 C.P9010, cdma2000 High Rate Packet Data Air Interface Specification, Ballot Resolution Version, September 12, 2000.
2. 3GPP2 C.P9011, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network, Dec.14, 2000.
3. 3GPP2 C.P9012, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Terminal, Dec.14, 2000.

Receivers for 1xEV Design Library

- *1xEV FwdChnlEstimate* (1xev)
- *1xEV FwdMRC* (1xev)
- *1xEV FwdReceiver* (1xev)
- *1xEV RevChnlEstimate* (1xev)
- *1xEV RevCohReceiver* (1xev)

1xEV_FwdChnlEstimate

Description: 1xEV Forward channel estimator
Library: 1xEV, Receivers
Class: SDF1xEV_FwdChnlEstimate

Parameters

Name	Description	Default	Symbol	Unit	Type	Range
MaxSearchPathNum	range for searching strongest paths	30			int	[K:K +100]
EstimateWindow	window size for estimating channel coefficients: HalfSlot, OneSlot	HalfSlot	N		enum	
FingerNumber	number of Rake receiver fingers	3	K		int	[1:6]
SampPerChip	number of samples per chip	4	R		int	[1:32]
FilterOrder	filter order	48	F		int	[12:50]

Pin Inputs

Pin	Name	Description	Signal Type
1	SigIn	received baseband signal.	complex
2	PN	input complex PN code	complex

Pin Outputs

Pin	Name	Description	Signal Type
3	CoeOut	output multipath channel coefficient for every finger.	complex
4	DlyOut	multipath delays for every finger.	int

Notes/Equations

1. This model estimates forward link channel profile, including delay, strength and phase of multipath. This model combines channel estimate and multipath search. The SampPerChip parameter specifies that the received signal is sampled at SampPerChip times the chip rate. The PN input is a product of the short PN code and Walsh function used by the pilot channel.
2. Channel estimation is carried out over the pilot channel. The estimated length is set by the EstimateWindow parameter.
3. Each firing, K DlyOut tokens, K CoeOut tokens, and one Pilot token are produced when (N+1)×1024×R SigIn tokens and (N+1)×1024×R PN tokens are consumed, where N=0 when EstimateWindow=HalfSlot, N=1 when EstimateWindow=OneSlot.

References

1. Urs Fawer, "A Coherent Spread-Spectrum Diversity-Receiver with AFC for Multipath Fading

Channels," *IEEE Trans. on Comm* . Vol.42, pp1300-1311, 1994.
2. A.J. Viterbi, Principles of Spread Spectrum Communication, The Peoples Posts & Telecommunications Publishing, 1995.
3. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_FwdMRC

Description: Forward Maximal Ratio Combiner
Library: 1xEV, Receivers
Class: SDF1xEV_FwdMRC

Parameters

Name	Description	Default	Symbol	Unit	Type	Range
EstimateWindow	window size for estimating channel coefficients: HalfSlot, OneSlot	HalfSlot			enum	
FingerNumber	number of Rake receiver fingers	3	K		int	[1:6]
SampPerChip	number of samples per chip	4	R		int	[1:32]
FilterOrder	filter order	48			int	[12:50]

Pin Inputs

Pin	Name	Description	Signal Type
1	SigIn	input received signal.	complex
2	CoeIn	input multipath channel coefficients	complex
3	DlyIn	input multipath delays	int

Pin Outputs

Pin	Name	Description	Signal Type
4	SigOut	output signals	complex

Notes/Equations

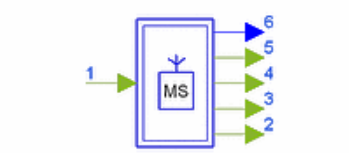
1. This model implements coherent receiving with maximal ratio combining (MRC). The necessary coefficients for rake combining, including multipath delay and channel phase and attenuation, are received from the channel estimator component; all parameters must remain consistent with 1xEV_FwdChnlEstimate.

   Each firing, (N+1)×1024 SigOut tokens are produced, (N+1)×1024×R SigIn tokens, (N+1)×1024 tokens of input PN, K tokens of DlyIn, K tokens of CoeIn are consumed, where N=0 when EstimateWindow=HalfSLot, N=1 when EstimateWindow=OneSlot.

References

1. Urs Fawer, "A Coherent Spread-Spectrum Diversity-Receiver with AFC for Multipath Fading Channels," *IEEE Trans. on Comm* . Vol.42, pp1300-1311, 1994.
2. A.J. Viterbi, *Principles of Spread Spectrum Communication* , The Peoples Posts & Telecommunications Publishing, 1995.
3. IS2000.2, *Physical Layer Standard for cdma2000 Spread Spectrum Systems* , April 1999.

1xEV_FwdReceiver



Description: 1xEV Foward link receiver subnetwork
Library: 1xEV, Receivers
Class: SDF1xEV_FwdReceiver

Parameters

Name	Description	Default	Symbol	Unit	Type	Range
DataRate	data rate of the forward traffic channel: R38.4kbps 16 slot, R76.8kbps 8 slot, R153.6kbps 4 slot, R307.2kbps 2 slot, R614.4kbps 1 slot, R307.2kbps 4 slot, R614.4kbps 2 slot, R1228.8kbps 1 slot, R921.6kbps 2 slot, R1843.2kbps 1 slot, R1228.8kbps 2 slot, R2457.6kbps 1 slot	R38.4kbps 16 slot			enum	
EstimateWindow	window size for estimating channel coefficients: HalfSlot, OneSlot	HalfSlot			enum	
FingerNumber	finger number of rake receiver	1	K		int	[1:6]
Q_Phase	sign of sine: Sine, Minus Sine	Minus Sine			enum	

Pin Inputs

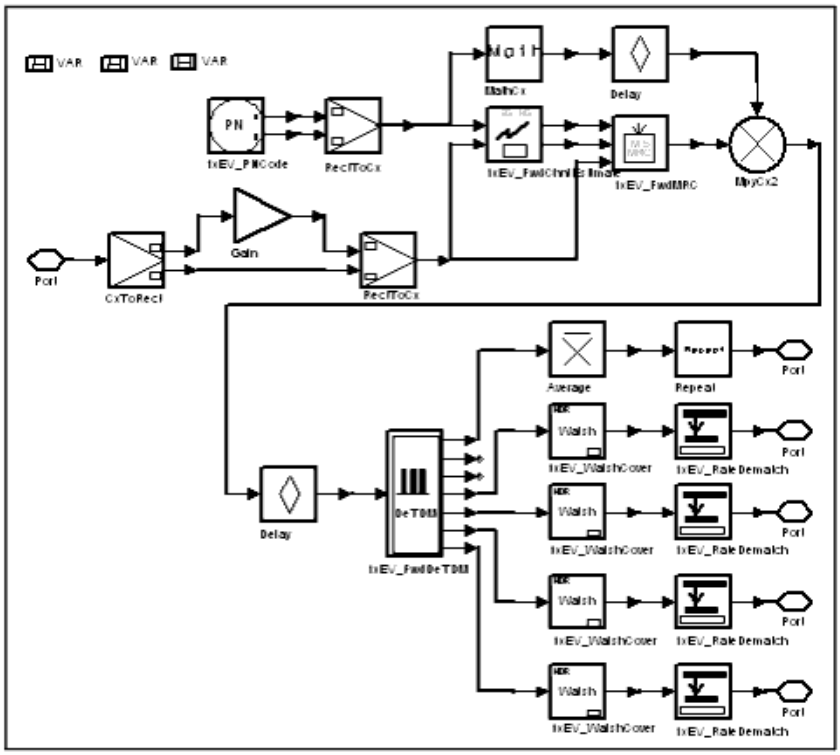
Pin	Name	Description	Signal Type
1	In	input data	complex

Pin Outputs

Pin	Name	Description	Signal Type
2	Data1	data from the first packet in the forward traffic channel or control channel	complex
3	Data2	data from the second packet in the forward traffic channel or control channel	complex
4	Data3	data from the third packet in the forward traffic channel or control channel	complex
5	Data4	data from the fourth packet in the forward traffic channel or control channel	complex
6	Pilot	pilot data	real

Notes/Equations

1. The subnetwork provides a 1xEV forward link receiver, which includes channel estimation, maximal ratio combining, DeTDM, fast hadamard transformation and rate dematching. The schematic is shown below.



1xEV_FwdReceiver Subnetwork

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_RevChnlEstimate

Description: Reverse link channel estimator
Library: 1xEV, Receivers
Class: SDF1xEV_RevChnlEstimate

Parameters

Name	Description	Default	Symbol	Unit	Type	Range
MaxSearchPathNum	range for searching strongest paths	30			int	[max(O/4:3*L):O/4+100]
SampPerChip	number of samples per chip	4	R		int	[1:32]
FilterOrder	filter order	48	O		int	[12:50]
FingerNumber	number of fingers in Rake receiver	3	L		int	[1:6]

Pin Inputs

Pin	Name	Description	Signal Type
1	SigIn	received signal	complex
2	PNp	pilot channel PN code	complex

Pin Outputs

Pin	Name	Description	Signal Type
3	CoeOut	amplitude and phase of each selected path	complex
4	DlyOut	delay spread of each selected path in terms of sample	int

Notes/Equations

1. This model estimates channel profile, including delay spread and strength and phase of multipath. Information is received from the pilot channel signal.

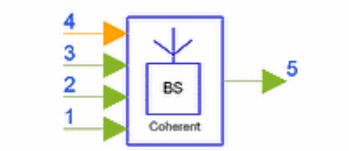
   Each firing, L CoeOut tokens and L DlyOut tokens are produced when 384×R SigIn tokens and 384×R PNp tokens are consumed.
2. Channel estimation is carried out over the pilot channel. On the reverse pilot channel, pilot signal and reverse rate indicator (RRI) symbols are transmitted. Pilot signal is known as am=1; RRI symbols are unknown. During the period of RRI symbols transmission, RRI symbol decisions will be fed back to estimate the channel parameters.

   Discrimination of the channel estimation is sampled. The strongest paths are selected and intervals between the selected paths are longer than a chip duration. The phases and attenuation factors of those paths and the corresponding delays are output and used by the Rake receiver.

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.
2. Li Yan, *Research of Synchronization Technique in Direct Sequence Spread Spectrum Communication System* , Ph.D. Dissertation, March, 1998.

1xEV_RevCohReceiver



Description: Reverse link Rake receiver
Library: 1xEV, Receivers
Class: SDF1xEV_RevCohReceiver

Parameters

Name	Description	Default	Symbol	Unit	Type	Range
SampPerChip	number of samples per chip	4	R		int	[1:32]
FingerNumber	number of fingers in Rake receiver	3	L		int	[1:6]
WalshLength	Walsh code length used for spreading	16	N		int	2^n, n=1,... ,8

Pin Inputs

Pin	Name	Description	Signal Type
1	SigIn	received signal	complex
2	PN	PN code used by corresponding channel	complex
3	CoeIn	amplitude and phase of each selected path	complex
4	DlyIn	delay spread of each selected path in terms of sample	int

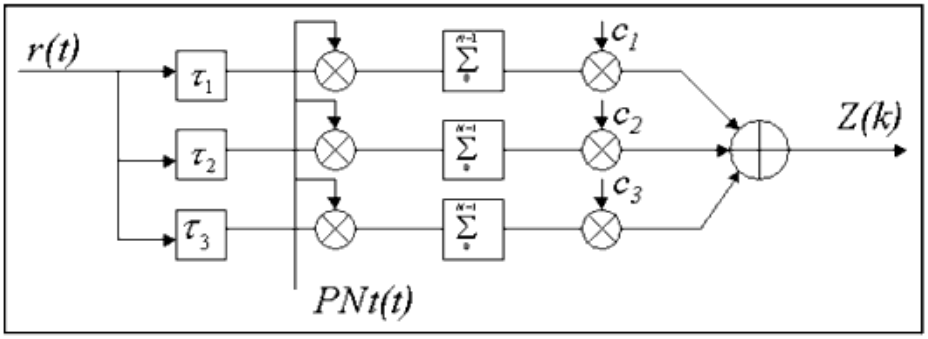
Pin Outputs

Pin	Name	Description	Signal Type
5	SigOut	output signal after maximal ratio combination	complex

Notes/Equations

1. This model performs maximal ratio combining by collecting the energy of the receiving arms. The phases and attenuation factors of those paths are inputs to this model.

   Each firing, 384/N SigOut tokens are produced when 384×R SigIn tokens, 384 PN tokens, L CoeIn tokens and L DlyIn are consumed.
2. For spread spectrum receivers, multi-path signals can be distinguished. A Rake receiver with maximal ratio combination is used, as illustrated in the following figure.



Rake Receiver Structure

In the figure, τ_l is delay of lth path, and c_l is the coefficient of lth path.

Let r(t) be the received signal, cl be the estimation of the selected multipaths, τ_l be the delay of the selected multipaths, then output Z(t) of maximal ratio combiner is

$$Z(t) = \sum_{l=0}^{L} c_l^* \int_{nT_b}^{(n+1)T_b} r(t+\tau_l) \times (PNt)^*(t)$$

where L=FingerNum.

The output of this model will be input to the decoder and de-interleaver to recover the original signal.

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

Signal Source Design Examples

Introduction

The 1xEV signal source workspace (1xEV_SignalSource_wrk) provides designs and verification solutions for 1xEV network and terminal access. Example designs included for this workspace are described in the following sections.

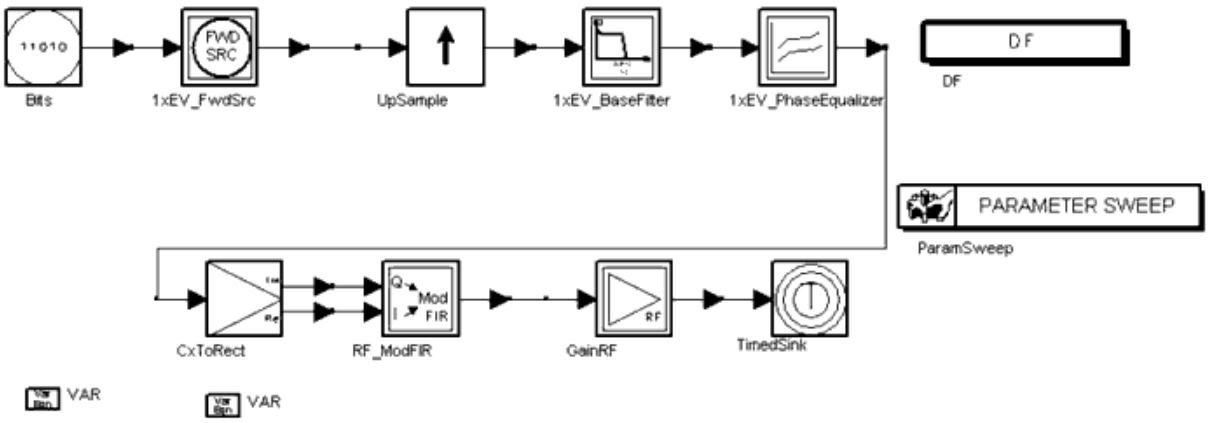
- DSN_1xEV_FwdCCDF for forward link CCDF measurement
- DSN_1xEV_FwdFreqDomainTest for forward link frequency domain measurement
- DSN_1xEV_FwdEVM for forward link EVM measurement
- DSN_1xEV_RevEVM for reverse link EVM measurement
- DSN_1xEV_FwdChTest for forward link spectrum, constellation, PAPR, and ACPR measurement
- DSN_1xEV_RevChTest for reverse link spectrum, constellation, PAPR, and ACPR measurement

Forward Link CCDF Measurement

- DSN_1xEV_FwdCCDF Design

Description

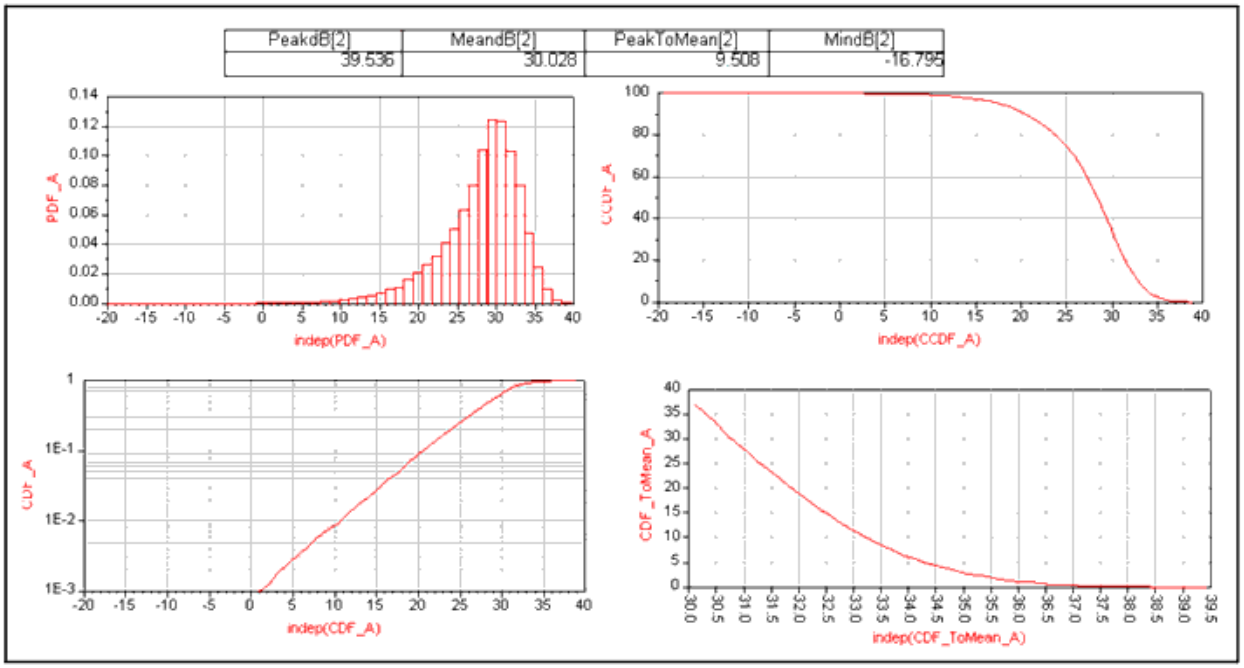
DSN_1xEV_FwdCCDF is used to measure the 1xEV/DO (data only mode) forward link CCDF. Three cases are swept: idle slot transmission, active/idle slot transmission with 50% duty cycle, and active slot transmission. QPSK modulation is used.
The schematic for this design is shown in the following figure. 1xEV_FwdSrc is the signal source of one user that can transmit up to 4 packets at the same time.



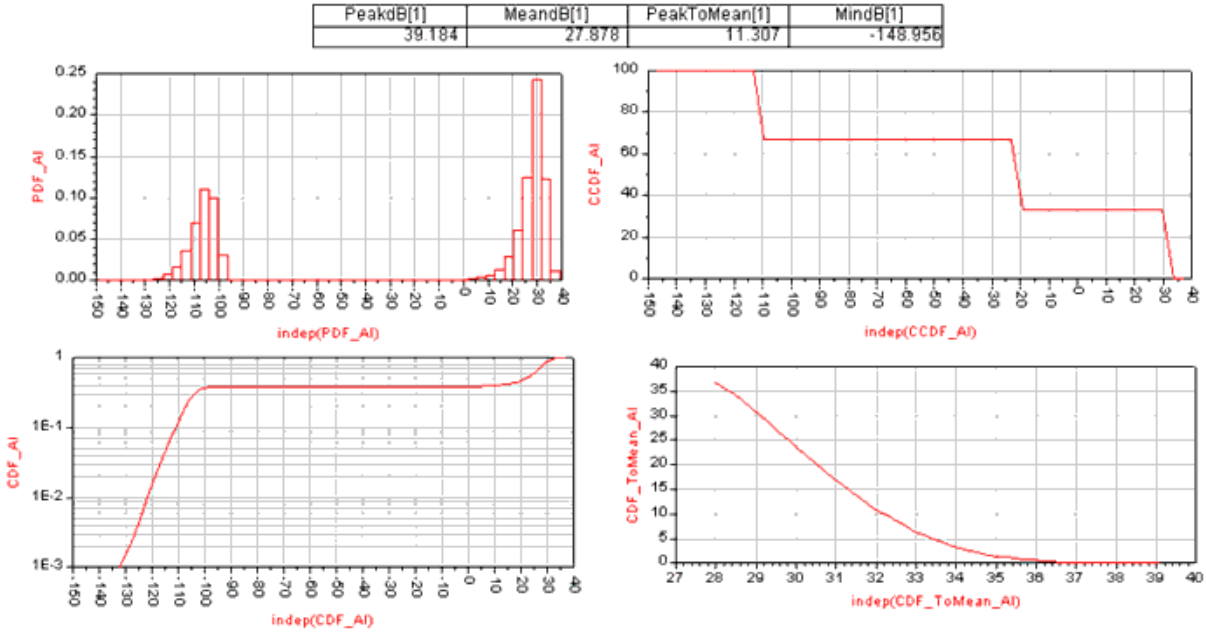
DSN_1xEV_FwdCCDF Schematic

Simulation Results

Simulation results displayed in DSN_1xEV_FwdCCDF.dds are shown in the following three figures. Page Equations shows the equations that are used for calculating the values of CCDF.

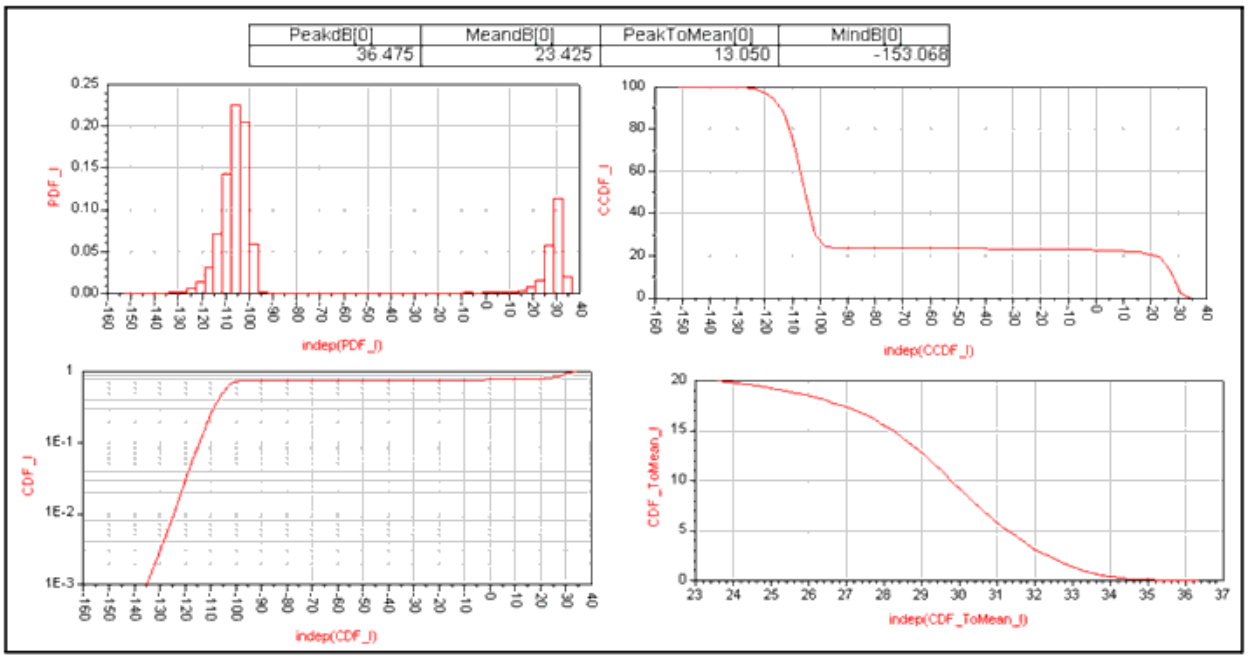


CCDF for 1xEV Systems in Active Slot Transmission



CCDF for 1xEV Systems in Active/Idle Slot Transmission

(50% Duty Cycle)



CCDF for 1xEV Systems in Idle Slot Transmission

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 2002
- Simulation Time: 155 seconds

References

1. 3GPP2 C.P9010, cdma2000 High Rate Packet Data Air Interface Specification, Ballot Resolution Version, September 12, 2000.
2. 3GPP2 C.P9011, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network, Dec. 14, 2000.
3. 3GPP2 C.P9012, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Terminal, Dec. 14, 2000.

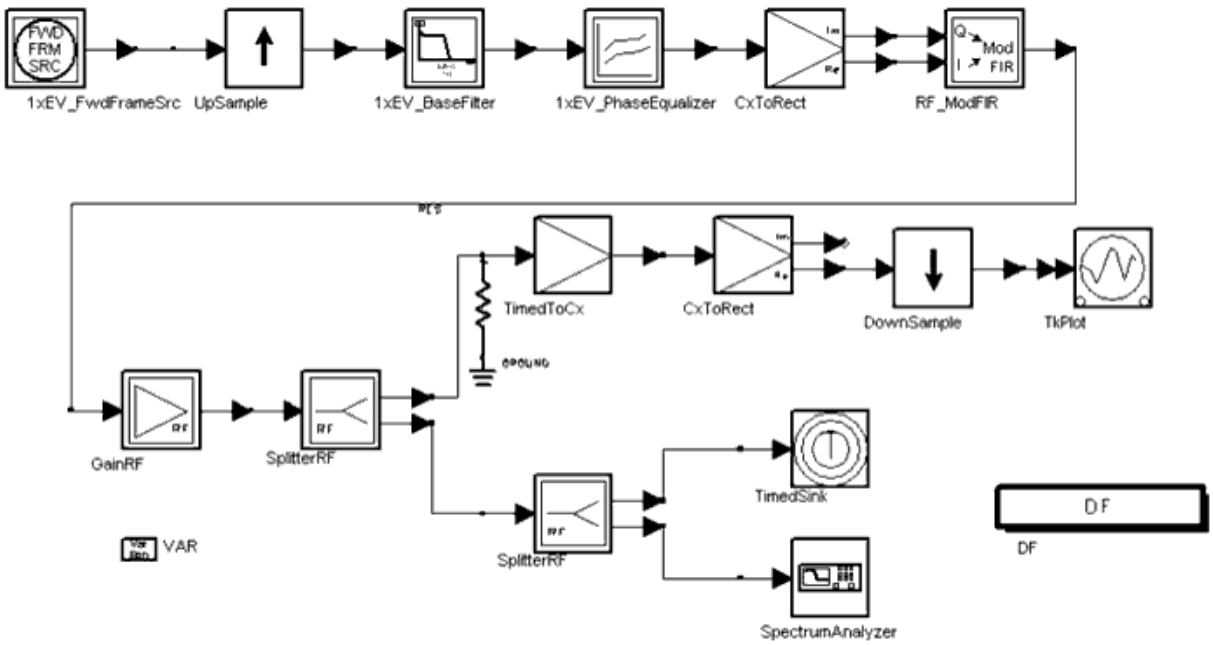
Forward Link Signal Source Measurement

- DSN_1xEV_FwdChTest Design

Description

DSN_1xEV_FwdChTest is used for forward link signal source spectrum, CCDF, peak average power ratio (PAPR), and adjacent channel power ratio (ACPR).

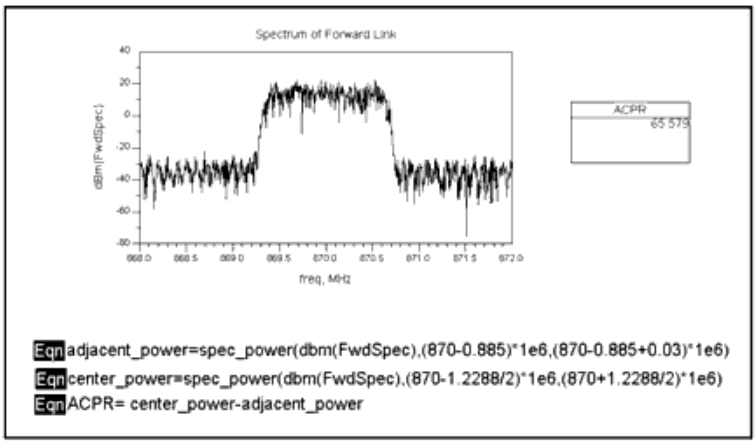
The schematic of this design is shown in the following figure. 1xEV_FwdFrameSrc is the signal source that generates 16 consecutive one-slot packets in the data frame format.



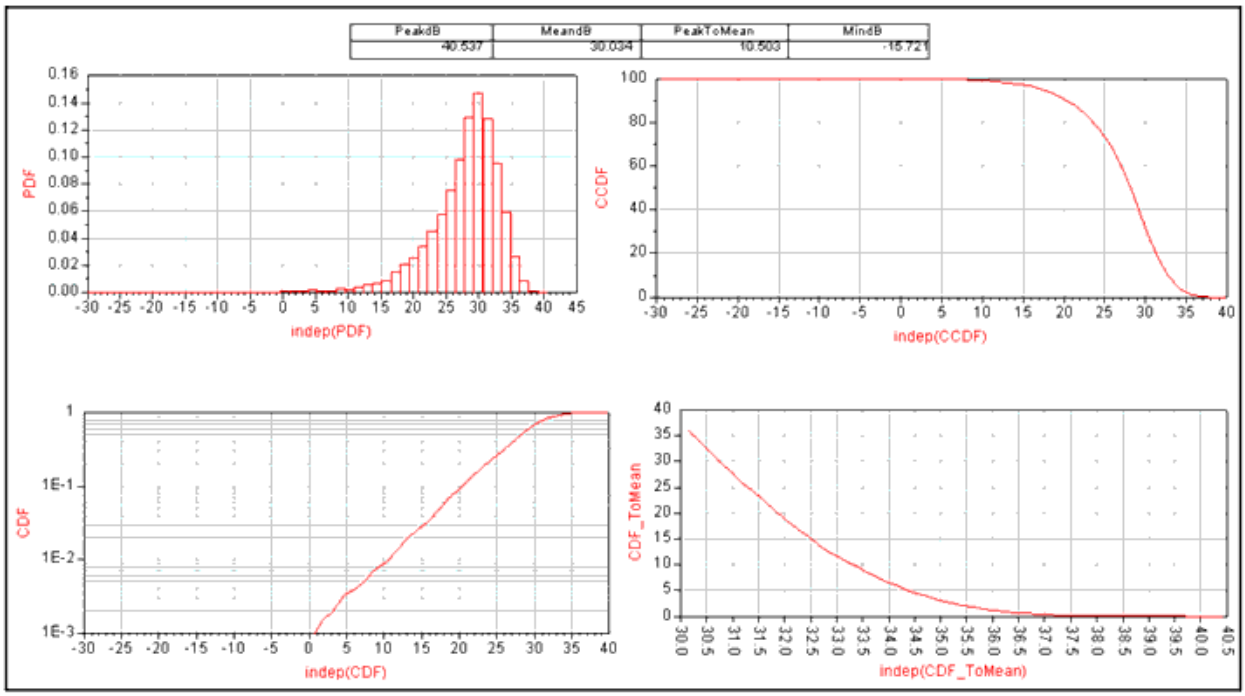
DSN_1xEV_FwdChTest Schematic

Simulation Results

Simulation results displayed in DSN_1xEV_FwdChTest.dds are shown in the following two figures.



Forward Link Signal Spectrum and ACPR



Forward Link Signal CCDF

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 2002
- Simulation Time: 270 seconds

References

1. 3GPP2 C.P9010, cdma2000 High Rate Packet Data Air Interface Specification, Ballot Resolution Version, September 12, 2000.
2. 3GPP2 C.P9011, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network, Dec. 14, 2000.
3. 3GPP2 C.P9012, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Terminal, Dec. 14, 2000.

Forward Link EVM Measurement

- DSN_1xEV_FwdEVM Design

Description

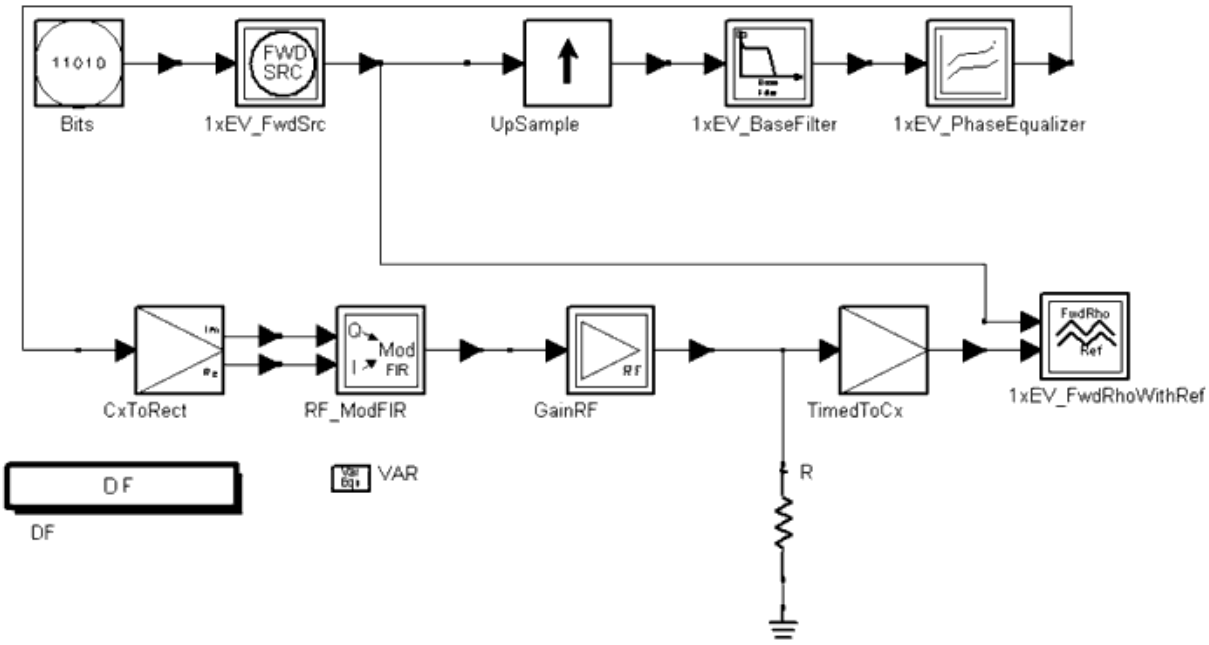
Modulation accuracy is the ability of the transmitter to generate the ideal signal. The error vector between the vector representing the transmitted signal and the vector representing the error-free modulated signal defines modulation accuracy. The magnitude of the error vector is called error vector magnitude (EVM).

The schematic for this design is shown in the following figure. 1xEV_FwdSrc generates the RF band signal for measurement. 1xEV_FwdRhoWithRef implements the EVM measurements.

The two data paths from the source to the measurement component are:

- one for the real transmitted signals that go through the device under test;
- one for the reference signals needed in the measurement.

Output variable EVM is the parameter to be tested.



DSN_1xEV_FwdEVM Schematic

Simulation Results

Simulation results displayed in DSN_1xEV_FwdEVM.dds are shown in the following figure.

EVM (Error Vector Magnitude) measurement result:

EVM
7.67547E-8

Forward Link EVM Simulation Results

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 2002
- Simulation Time: 140 seconds

References

1. 3GPP2 C.P9010, cdma2000 High Rate Packet Data Air Interface Specification, Ballot Resolution Version, September 12, 2000.
2. 3GPP2 C.P9011, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network, Dec.14, 2000.
3. 3GPP2 C.P9012, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Terminal, Dec. 14, 2000.

Forward Link Frequency Domain Test

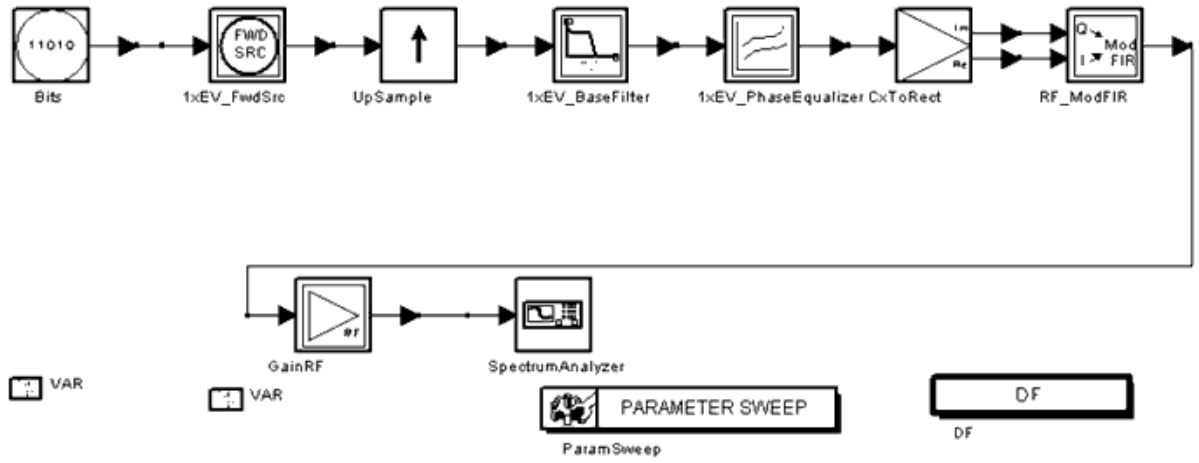
- DSN_1xEV_FwdFreqDomainTest Design

Description

DSN_1xEV_FwdFreqDomainTest is used for measuring the forward link spectrum, occupied bandwidth, channel power in 1xEV/DO (data only mode). Three modulation types (QPSK, 8PSK, 16QAM) with five transmission modes (idle slot, active slot, and active/idle slot transmission with 25%, 50%, and 75% duty cycles) are swept.

- case 1: idle slot transmission, QPSK modulation
- case 2: idle slot transmission, 8PSK modulation
- case 3: idle slot transmission, 16QAM modulation
- case 4: active/ idle slot transmission with 25% duty cycle, QPSK modulation
- case 5: active/idle slot transmission with 25%duty cycle, 8PSK modulation
- case 6: active/idle slot transmission with 25% duty cycle, 16QAM modulation
- case 7: active/idle slot transmission with 50% duty cycle, QPSK modulation
- case 8: active/idle slot transmission with 50% duty cycle, 8PSK modulation
- case 9: active/idle slot transmission with 50% duty cycle, 16QAM modulation
- case 10: active/idle slot transmission with 75% duty cycle, QPSK modulation
- case 11: active/idle slot transmission with 75% duty cycle, 8PSK modulation
- case 12: active/idle slot transmission with 75% duty cycle, 16QAM modulation
- case 13: active slot transmission, QPSK modulation
- case 14: active slot transmission, 8PSK modulation
- case 15: active slot transmission, 16QAM modulation

The schematic for this design is shown in the following figure. 1xEV_FwdSrc is the signal source of one user that can transmit up to 4 packets at the same time.

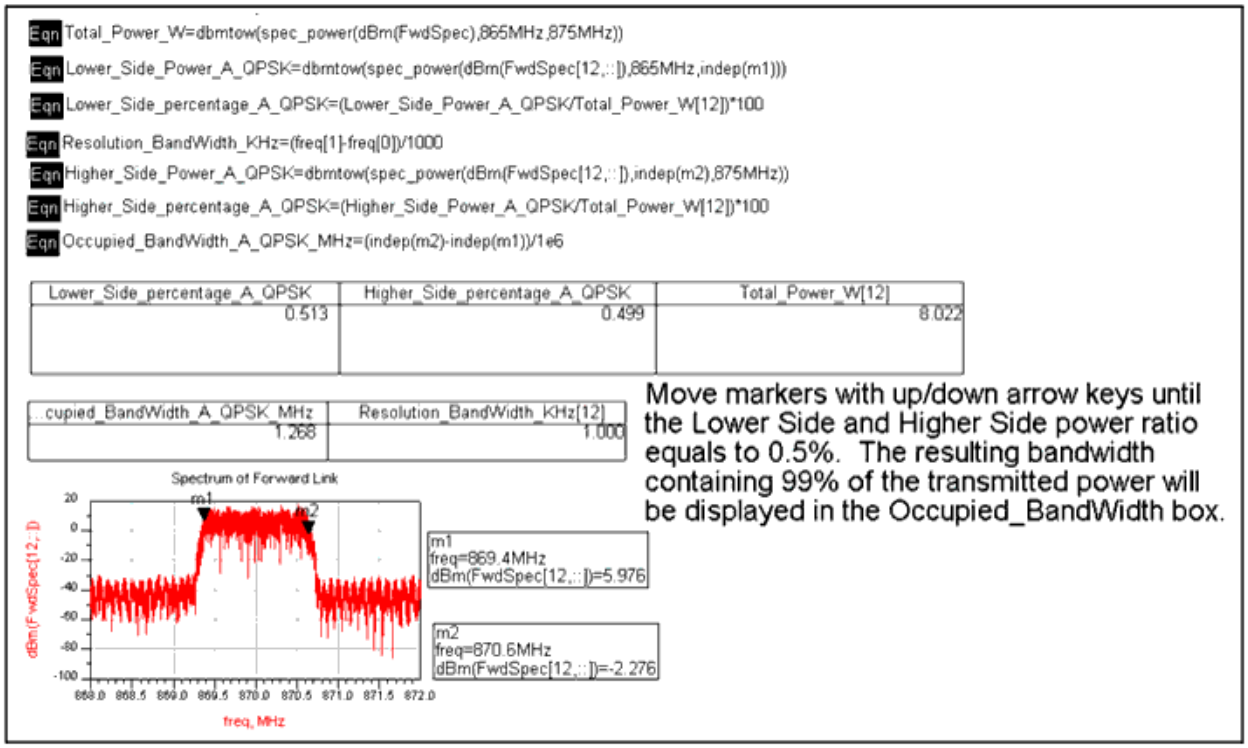


DSN_1xEV_FwdFreqDomainTest Schematic

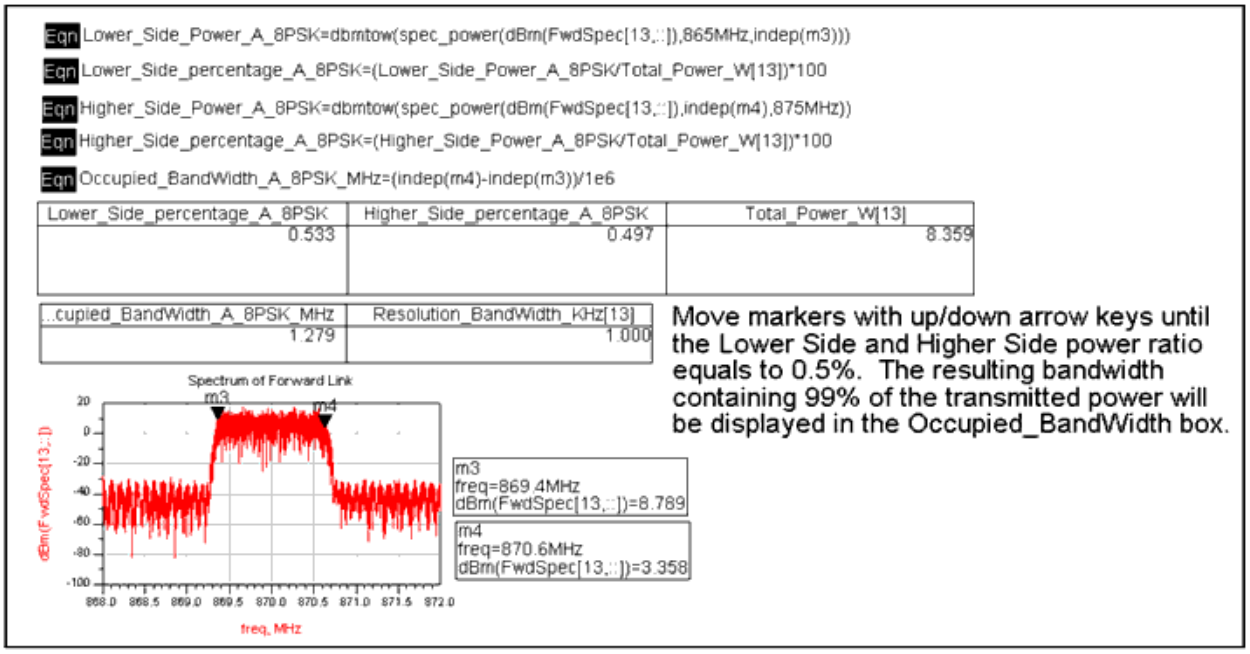
Simulation Results

Simulation results displayed in DSN_1xEV_FwdFreqDomainTest.dds are shown in the following eight

figures.



Forward Link Spectrum with QPSK Modulation



Forward Link Spectrum with 8PSK Modulation

Eqn Lower_Side_Power_A_16QAM=dbmtow(spec_power(dBm(FwdSpec[14,::]),865MHz,indep(m5)))

Eqn Lower_Side_percentage_A_16QAM=(Lower_Side_Power_A_16QAM/Total_Power_W[14])*100

Eqn Higher_Side_Power_A_16QAM=dbmtow(spec_power(dBm(FwdSpec[14,::]),indep(m6),875MHz))

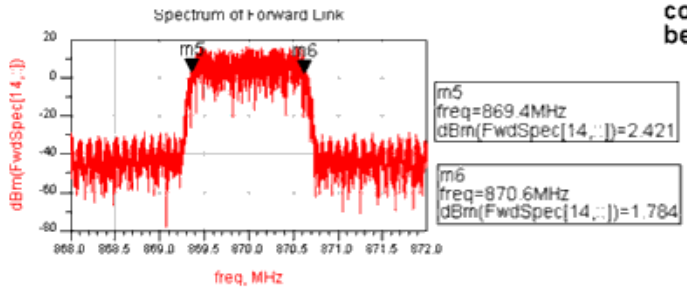
Eqn Higher_Side_percentage_A_16QAM=(Higher_Side_Power_A_16QAM/Total_Power_W[14])*100

Eqn Occupied_BandWidth_A_16QAM_MHz=(indep(m6)-indep(m5))/1e6

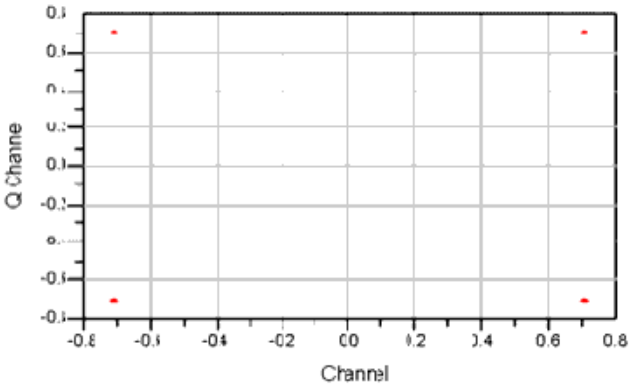
Lower_Side_percentage_A_16QAM	Higher_Side_percentage_A_16QAM	Total_Power_W[14]
0.498	0.504	8.369

...pied_BandWidth_A_16QAM_MHz	Resolution_BandWidth_KHz[14]
1.265	1.000

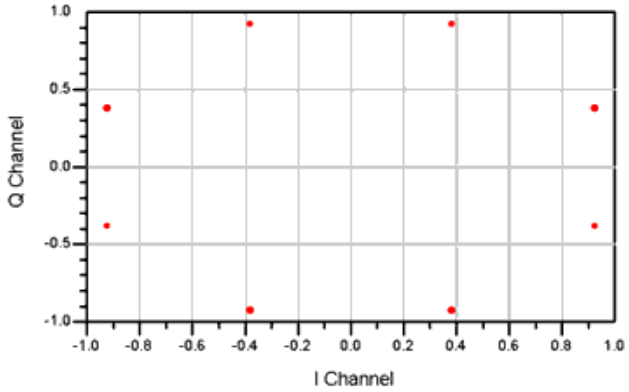
Move markers with up/down arrow keys until the Lower Side and Higher Side power ratio equals to 0.5%. The resulting bandwidth containing 99% of the transmitted power will be displayed in the Occupied_BandWidth box.



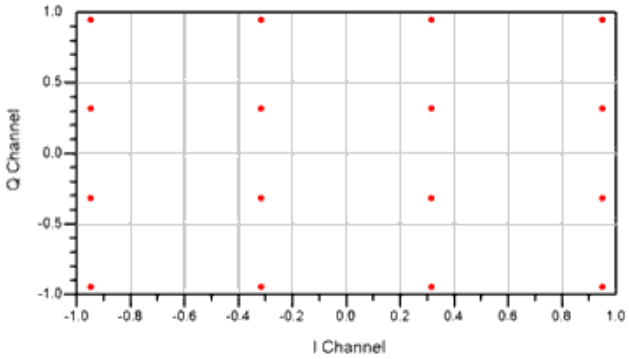
Forward Link Spectrum with 16QAM Modulation



Forward Link Constellation with QPSK Modulation



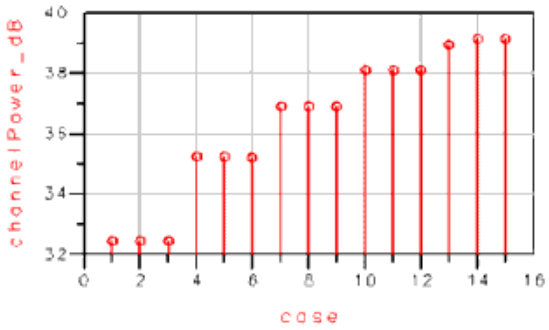
Forward Link Constellation with 8PSK Modulation



Forward Link Constellation with 16QAM Modulation

Eqn channelPower_dB=spec_power(dBm(FwdSpec),(870-1.25/2)*1e6Hz, (870+1.25/2)*1e6Hz)

case	channelPower_dB
1.000	32.463
2.000	32.459
3.000	32.464
4.000	35.239
5.000	35.240
6.000	35.232
7.000	36.918
8.000	36.913
9.000	36.915
10.000	38.120
11.000	38.116
12.000	38.128
13.000	38.974
14.000	39.148
15.000	39.165

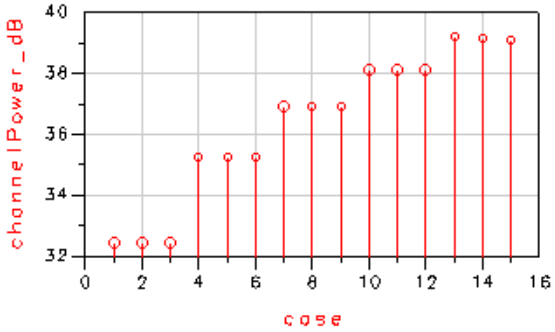


Forward Link Channel Power

Channel Power of 1xEV Forward Link

Eqn channelPower_dB=spec_power(dBm(FwdSpec),(870-1.25/2)*1e6Hz, (870+1.25/2)*1e6Hz)

case	...nnelPower_dB
1.000	32.459
2.000	32.467
3.000	32.452
4.000	35.242
5.000	35.235
6.000	35.237
7.000	36.923
8.000	36.904
9.000	36.911
10.000	38.136
11.000	38.112
12.000	38.133
13.000	39.191
14.000	39.126
15.000	39.084



Forward Link Channel Power

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 2002
- Simulation Time: 2250 seconds

References

1. 3GPP2 C.P9010, cdma2000 High Rate Packet Data Air Interface Specification, Ballot Resolution Version, September 12, 2000.
2. 3GPP2 C.P9011, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network, Dec. 14, 2000.
3. 3GPP2 C.P9012, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Terminal, Dec. 14, 2000.

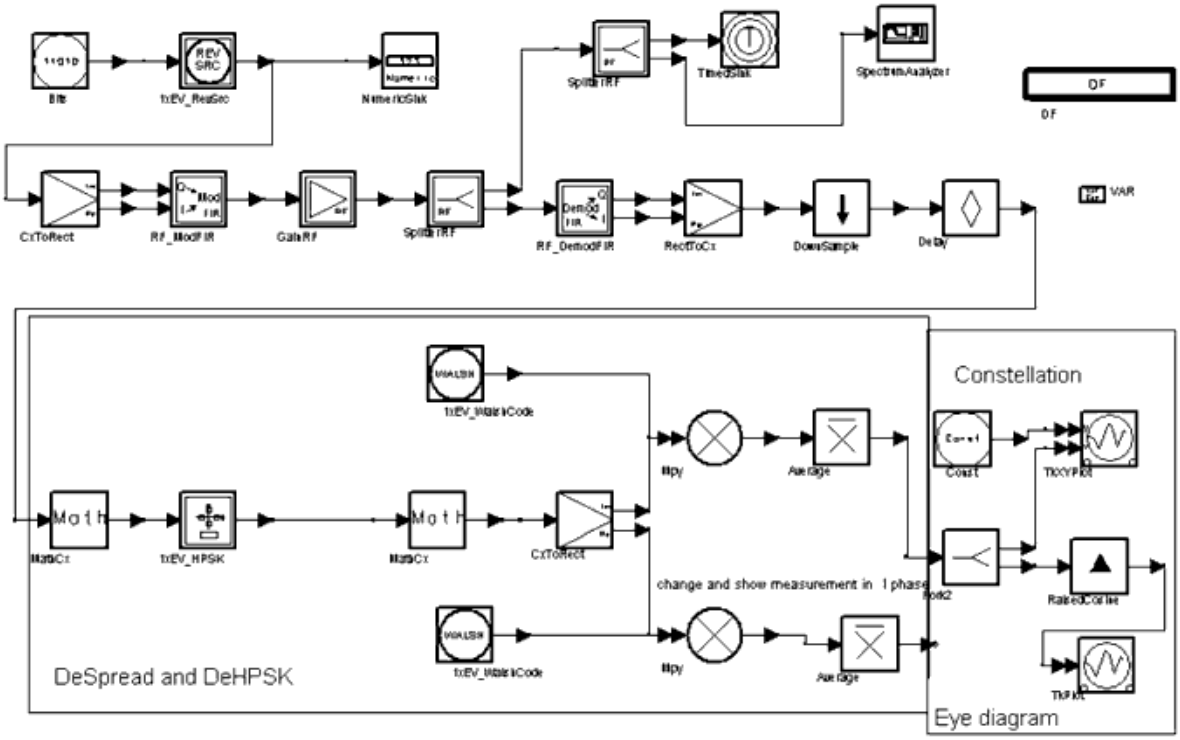
Reverse Link Signal Source Measurement

- DSN_1xEV_RevChTest Design

Description

DSN_1xEV_RevChTest is used to measure the reverse link signal source spectrum, constellation, CCDF of peak average power ratio (PAPR), and adjacent channel power ratio (ACPR).

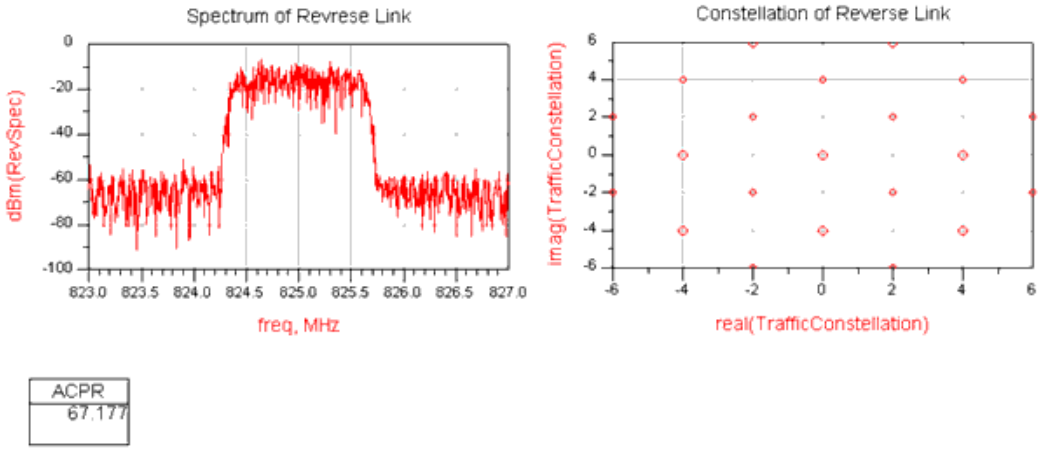
The schematic for this design is shown in the following figure. 1xEV_RevSrc is the signal source of one user that can transmit up to 4 packets at the same time.



DSN_1xEV_RevChTest Schematic

Simulation Results

Simulation results displayed in DSN_1xEV_RevChTest.dds are shown in the following two figures.

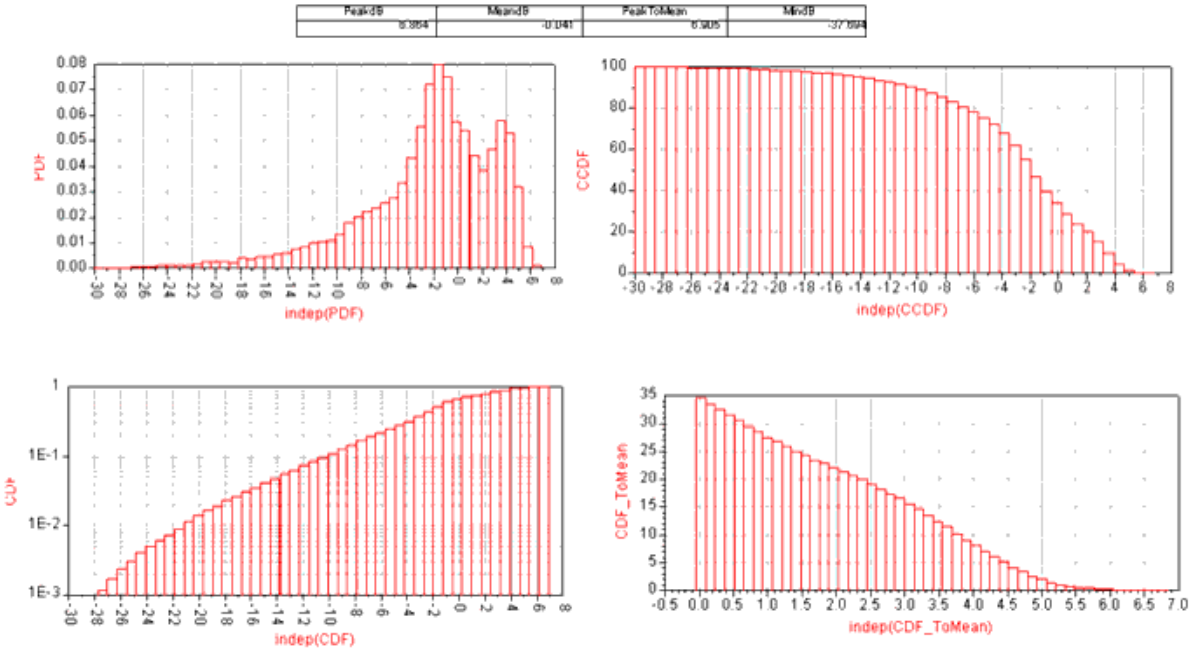


Eqn adjacent_power=spec_power(dbm(RevSpec),(825-0.885)*1e6,(825-0.885+0.03)*1e6)

Eqn center_power=spec_power(dbm(RevSpec),(825-1.2288/2)*1e6,(825+1.2288/2)*1e6)

Eqn ACPR= center_power-adjacent_power

Reverse Link Signal Spectrum, Constellation, and ACPR



Reverse Link Signal CCDF

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 2002
- Simulation Time: 200 seconds

References

1. 3GPP2 C.P9010, cdma2000 High Rate Packet Data Air Interface Specification, Ballot Resolution Version, September 12, 2000.
2. 3GPP2 C.P9011, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network, Dec. 14, 2000.
3. 3GPP2 C.P9012, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Terminal, Dec. 14, 2000.

Reverse Link EVM Measurement

- DSN_1xEV_RevEVM Design

Description

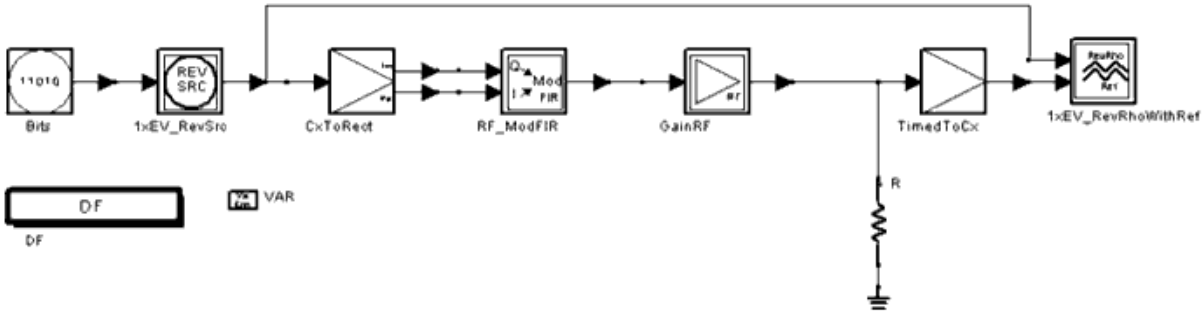
Modulation accuracy is the ability of the transmitter to generate the ideal signal. The error vector between the vector representing the transmitted signal and the vector representing the error-free modulated signal defines modulation accuracy. The magnitude of the error vector is called error vector magnitude (EVM).

The figure below shows the schematic for this design. 1xEV_RevSrc generates RF band signal for measurement. The 1xEV_RevRhoWithRef subnetwork implements the EVM measurements.

The two data paths from the source to the measurement component are:

- one for the real transmitted signals which go through the device under test;
- one for the reference signals needed in the measurement.

The output variable EVM is the parameter to be tested.



DSN_1xEV_RevEVM Schematic

Simulation Results

Simulation results displayed in DSN_1xEV_RevEVM.dds are shown in the following figure.

EVM
2.23675E-6

Reverse Link EVM Simulation Results

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 1.5
- Simulation Time: approximately 100 seconds

References

1. 3GPP2 C.P9010, cdma2000 High Rate Packet Data Air Interface Specification, Ballot Resolution Version, September 12, 2000.
2. 3GPP2 C.P9011, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network, Dec. 14, 2000.
3. 3GPP2 C.P9012, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Terminal, Dec. 14, 2000

Signal Sources for 1xEV Design Library

- *1xEV FwdFrameSrc* (1xev)
- *1xEV FwdSrc* (1xev)
- *1xEV MAC Src* (1xev)
- *1xEV RevSrc* (1xev)

1xEV_FwdFrameSrc

Description: 1xEV forward link signal source in the format of data frame
Library: 1xEV, Signal Sources
Class: SDF1xEV_FwdFrameSrc

Parameters

Name	Description	Default	Unit	Type	Range
SlotStatus	state of each slot in the frame: All On, DutyCycle75, DutyCycle50, DutyCycle25, All Off, UserDefinedStatus	All On		enum	
ModType	modulation type for each slot: All QPSK, All 8PSK, All 16QAM, UserDefinedType	All QPSK		enum	
Slot1ModType	Status of the first slot: Mod_QPSK1, Mod_8PSK1, Mod_16QAM1, Inactive1	Mod_QPSK1		enum	
Slot2ModType	Status of the second slot: Mod_QPSK2, Mod_8PSK2, Mod_16QAM2, Inactive2	Mod_QPSK2		enum	
Slot3ModType	Status of the third slot: Mod_QPSK3, Mod_8PSK3, Mod_16QAM3, Inactive3	Mod_QPSK3		enum	
Slot4ModType	Status of the third slot: Mod_QPSK4, Mod_8PSK4, Mod_16QAM4, Inactive4	Mod_QPSK4		enum	
Slot5ModType	Status of the fourth slot: Mod_QPSK5, Mod_8PSK5, Mod_16QAM5, Inactive5	Mod_QPSK5		enum	
Slot6ModType	Status of the sixth slot: Mod_QPSK6, Mod_8PSK6, Mod_16QAM6, Inactive6	Mod_QPSK6		enum	
Slot7ModType	Status of the seventh slot: Mod_QPSK7, Mod_8PSK7, Mod_16QAM7, Inactive7	Mod_QPSK7		enum	
Slot8ModType	Status of the eighth slot: Mod_QPSK8, Mod_8PSK8, Mod_16QAM8, Inactive8	Mod_QPSK8		enum	
Slot9ModType	Status of the ninth slot: Mod_QPSK9, Mod_8PSK9, Mod_16QAM9, Inactive9	Mod_QPSK9		enum	
Slot10ModType	Status of the tenth slot: Mod_QPSK10, Mod_8PSK10, Mod_16QAM10, Inactive10	Mod_QPSK10		enum	
Slot11ModType	Status of the eleventh slot: Mod_QPSK11, Mod_8PSK11, Mod_16QAM11, Inactive11	Mod_QPSK11		enum	
Slot12ModType	Status of the twelfth slot: Mod_QPSK12, Mod_8PSK12, Mod_16QAM12, Inactive12	Mod_QPSK12		enum	
Slot13ModType	Status of the thirteenth slot: Mod_QPSK13, Mod_8PSK13, Mod_16QAM13, Inactive13	Mod_QPSK13		enum	
Slot14ModType	Status of the fourteenth slot: Mod_QPSK14, Mod_8PSK14, Mod_16QAM14, Inactive14	Mod_QPSK14		enum	
Slot15ModType	Status of the fifteenth slot: Mod_QPSK15, Mod_8PSK15, Mod_16QAM15, Inactive15	Mod_QPSK15		enum	
Slot16ModType	Status of the sixteenth slot: Mod_QPSK16, Mod_8PSK16, Mod_16QAM16, Inactive16	Mod_QPSK16		enum	
RA_Enable	enable or disable RA channel: RA_Yes, RA_No	RA_Yes		enum	
RAB_Length	the number of slots over which the Reverse Activity Bit is transmitted	8		int	{8, 16, 32, 64}
RPC_Enable	enable or disable RPC channel: RPC_Yes, RPC_No	RPC_Yes		enum	
RPC_ChNum	number of the reverse power control channel	1		int	[1:58]
RPC_ChSelect	the way to set channel index of reverse power control channel: Sequential, Random, UserDefined	Sequential		enum	
RPC_Index	user-defined RPC index	5		int array	[5:63]
RPC_Value	value of RPC bit in each RPC channel: All 0s, All 1s, Random Value	All 0s		enum	
Version	version of cdma2000 High Rate Packet Data Air Interface Specification: C_P9010, C_S0024	C_P9010		enum	
DRC_LockEnable	enable or disable DRCLock channel: DRC_LockYes, DRC_LockNo	DRC_LockYes		enum	
DRC_LockLength	the number of times that a DRCLock bit is repeated: _4_Times, _8_Times, _16_Times, _32_Times	_8_Times		enum	
DRC_LockPeriod	the time interval in units of slots between transmission of two consecutive DRCLock bit: _8_Slots, _16_Slots	_8_Slots		enum	

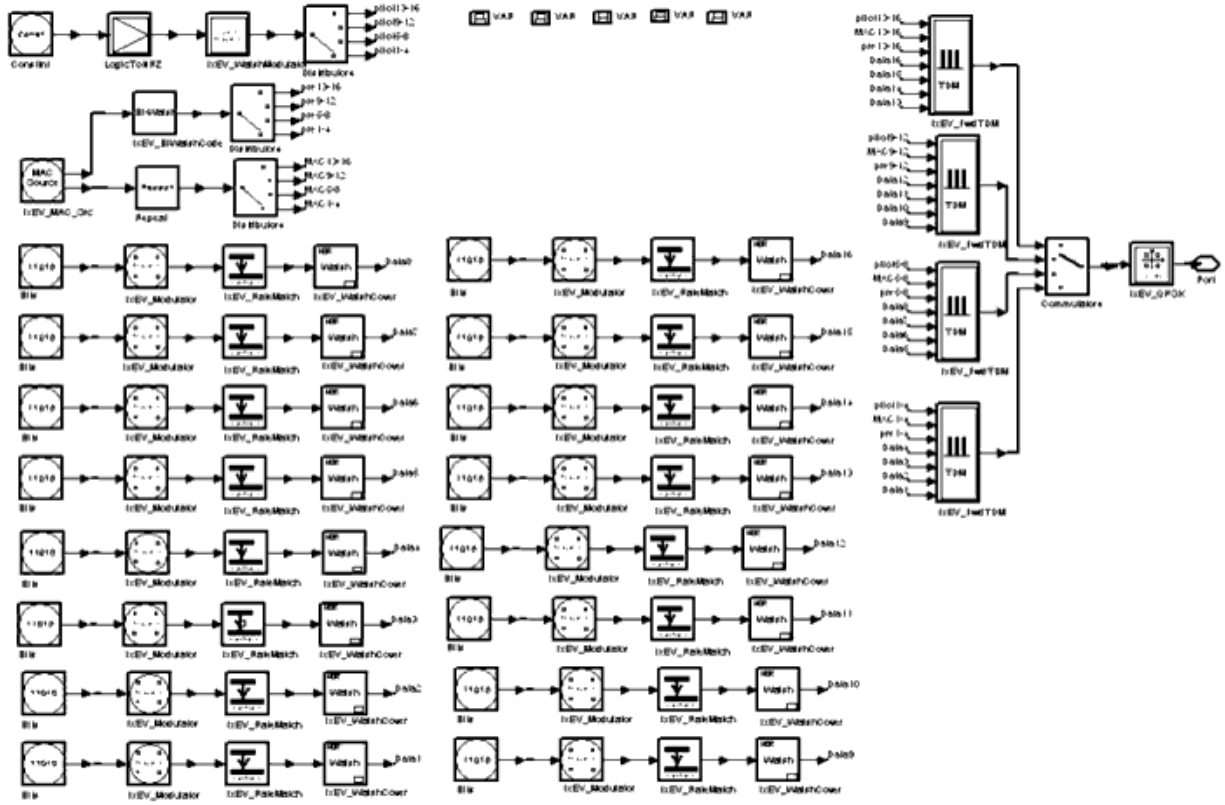
Pin Outputs

Pin	Name	Description	Signal Type
1	Output	Output	complex

Notes/Equations

1. This subnetwork is used to generate forward link source signal in the frame format. The forward channel consists of time-multiplexed channels: pilot channel, forward medium access control (MAC) channel, and forward traffic or control channel. The traffic channel carries user physical layer packets.

   The schematic for this subnetwork is shown in the following figure.
2. The forward link consists of slots of length 2048 chips (1.666...ms). Groups of 16 slots are aligned to the PN rolls of the zero-offset PN sequences.
3. The pilot channel consists of all-0 symbols transmitted on the I channel with Walsh cover 0. Each slot is divided into two half slots, each containing a pilot burst. Each pilot burst has a duration of 96 chips and is centered at the midpoint of the half slot.
4. The MAC channel consists of subchannels: reverse power control (RPC) channel and reverse activity (RA) channel. The RA channel transmits a reverse link activity bit (RAB) stream. Each MAC channel symbol is BPSK-modulated on one of 64 64-ary Walsh codewords (covers). The MAC symbol Walsh covers are transmitted four times per slot in bursts of 64 chips each.
5. The forward traffic channel is a packet-based, variable-rate channel. Data is fed into a QPSK/8PSK/16QAM modulator. The modulated symbol sequences are repeated and punctured as necessary. The resulting sequences of modulation symbols are demultiplexed to form 16 pairs (in-phase and quadrature) of parallel streams. Each parallel stream is covered with a distinct 16-ary Walsh function at a chip rate to yield Walsh symbols at 76.8 ksps. The Walsh-coded symbols of all streams are summed together to form a single in-phase stream and a single quadrature stream at a chip rate of 1.2288 Mcps.
6. Chips are time-division multiplexed with the preamble, pilot channel, and MAC channel chips to form the resultant sequence of chips for the quadrature spreading operation.
7. Sixteen consecutive slots are generated from this component, which is a whole frame. One-slot version packet is applied so that 16 consecutive slots are 16 packets, which provides flexibility in configuring each slot.
   Common modulation patterns and duty cycles are available by setting SlotStatus and ModType parameters. The modulation type of each slot in the frame can be set independently.
8. This model supports DRCLock channel when the Version parameter is set to C_S0024; otherwise DRCLock channel is not supported and only RPC channel bits are transmitted.



1xEV_FwdFrameSrc

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_FwdSrc

Description: Forword link signal generator
Library: 1xEV, Signal Sources
Class: SDF1xEV_FwdSrc

Parameters

Name	Description	Default	Unit	Type	Range
DataRate	data rate of the forward traffic channel: R38.4kbps 16 slot, R76.8kbps 8 slot, R153.6kbps 4 slot, R307.2kbps 2 slot, R614.4kbps 1 slot, R307.2kbps 4 slot, R614.4kbps 2 slot, R1228.8kbps 1 slot, R921.6kbps 2 slot, R1843.2kbps 1 slot, R1228.8kbps 2 slot, R2457.6kbps 1 slot	R38.4kbps 16 slot		enum	
SlotState	state of each slot: 0 for idle, 1 for active	1 0 0 0		int array	
Version	version of cdma2000 High Rate Packet Data Air Interface Specification: C_P9010, C_S0024	C_P9010		enum	

Pin Inputs

Pin	Name	Description	Signal Type
1	Input	input signal	int

Pin Outputs

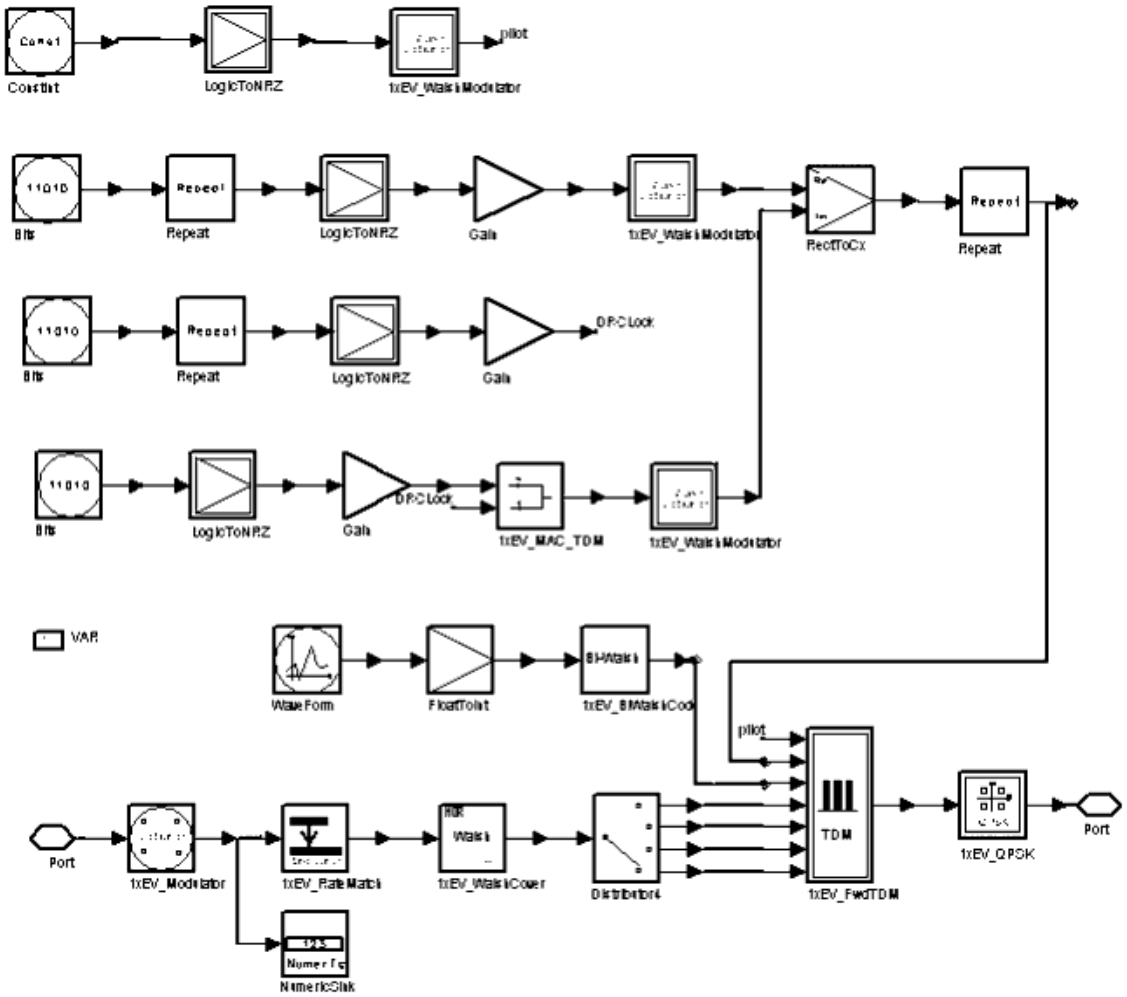
Pin	Name	Description	Signal Type
2	Output	output signal	complex

Notes/Equations

1. This subnetwork is used to generate forward link source signal.

   The schematic for this subnetwork is shown in the figure below.

   The forward channel consists of time-multiplexed channels: pilot channel, forward medium access control (MAC) channel, and forward traffic channel or control channel. The traffic channel carries user physical layer packets.
2. Each firing, four consecutive slots are generated. The status of the slot can be set to idle or active in the SlotState parameter.
3. This subnetwork supports DRCLock channel when the Version parameter is set to C_S0024; otherwise, the 1xEV_MAC_TDM used in this subnetwork only copies the input to the output.



1xEV_FwdSrc Schematic

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_MAC_Src

Description: Signal source for MAC channel
Library: 1xEV, Signal Sources
Class: SDF1xEV_MAC_Src

Parameters

Name	Description	Default	Unit	Type	Range
RA_Enable	enable or disable RA channel: RA_Yes, RA_No	RA_Yes		enum	
RAB_Length	the number of slots over which the Reverse Activity Bit is transmitted	8		int	{8, 16, 32, 64}
RPC_Enable	enable or disable RPC channel: RPC_Yes, RPC_No	RPC_Yes		enum	
RPC_ChNum	number of the reverse power control channel	1		int	[1:58]
RPC_ChSelect	the way to set channel index of reverse power control channel: Sequential, Random, UserDefined	Sequential		enum	
RPC_Index	user-defined RPC index	5		int array	[5:63] when RPC_ChSelect=UserDefined
RPC_Value	value of RPC bit in each RPC channel: All 0s, All 1s, Random Value	Random Value		enum	
Version	version of cdma2000 High Rate Packet Data Air Interface Specification: C_P9010, C_S0024	C_P9010		enum	
DRC_LockEnable	enable or disable DRCLock channel: DRC_LockYes, DRC_LockNo	DRC_LockYes		enum	
DRC_LockLength	the number of times that a DRCLock bit is repeated: _4_Times, _8_Times, _16_Times, _32_Times	_8_Times		enum	
DRC_LockPeriod	the time interval in units of slots between transmission of two consecutive DRCLock bit: _8_Slots, _16_Slots	_8_Slots		enum	

Pin Outputs

Pin	Name	Description	Signal Type
1	output	MAC signal in forward link	complex
2	MAC_Ix	MAC index	int

Notes/Equations

1. This model is signal source for MAC channel in forward link.

   Each firing, one MAC_Ix and 64 output tokens are produced.
2. The forward MAC Channel is composed of Walsh channels that are orthogonally covered and BPSK modulated on an in-phase or quadrature phase of the carrier. Each Walsh channel is identified by a MAC_Ix value of 0 to 63 and defines a unique 64-ary Walsh cover and a unique modulation

phase. The Walsh functions assigned to MAC_Ix values are:

$W_{i/2}^{64}$ for i = 0, 2, ..., 62

$W_{(i-1)/2}^{64}$ for i = 1,3, ..., 63

where i is the MAC_Ix value.

MAC channels with even-numbered MAC_Ix values are assigned to the in-phase (I) modulation phase, while those with odd-numbered MAC_Ix values are assigned to the quadrature (Q) modulation phase.

The MAC symbol Walsh covers are transmitted four times per slot in bursts of length 64 chips each. These bursts are transmitted before and after the pilot bursts of each slot.

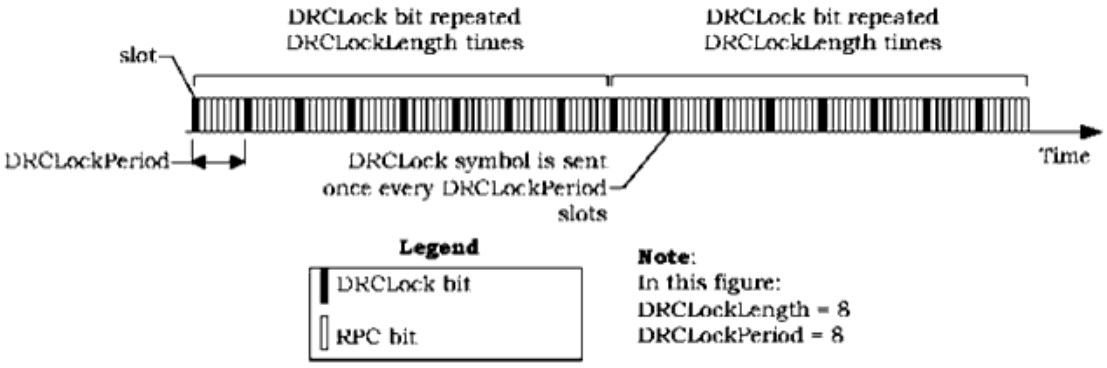
The MAC channel and Preamble use according to MAC_Ix are listed in the table below.

Symbols of each MAC Channel are transmitted on one of the Walsh channels. MAC channel gains may vary the relative power as a function of time. The orthogonal Walsh channels are scaled to maintain a constant total transmit power. The sum of the squares of the normalized gains on the orthogonal MAC Channels equal one.

MAC Channel and Preamble Use

MACIndex	MAC Channel Use	Preamble Use
0 and 1	Not Used	Not Used
2	Not Used	76.8-kbps Control Channel
3	Not Used	38.4-kbps Control Channel
4	RA Channel	Not Used
5-63	Available for RPC Channel Transmissions	Available for Forward Traffic Channel Transmissions

3. The reverse activity (RA) channel transmits the reverse activity bit (RAB) stream over the MAC channel with MACIndex 4. The RA bit is transmitted over RABLength successive slots. The RA channel data rate is 600/RABLength bps. Each RA bit is repeated and transmitted over RABLength consecutive slots. The RA bit in each slot is repeated to form four symbols per slot for transmission.
4. The RPC Channel and the DRCLock Channel will be time-division multiplexed and transmitted on the same MAC Channel. The RPC Channel will be transmitted in DRCLockPeriod-1 slots out of every DRCLockPeriod slot, where DRCLockPeriod is given as public data by the Forward Traffic Channel MAC Protocol. The RPC data rate will be 600 × (1 - 1/DRCLockPeriod) bps.
5. The DRCLock Channel will be transmitted in one out of every DRCLockPeriod slot. Each DRCLock bit will be repeated and transmitted in DRCLockLength slots, where DRCLockLength is given as public data by the Forward Traffic Channel MAC Protocol. The DRCLock data rate will be 600/(DRCLockLength × DRCLockPeriod) bps.
6. An example for the transmission of DRCLock bits with DRCLockLength equal to 8 and DRCLockPeriod equal to 8 is shown in the following figure.



DRCLock Puncturing Example

7. This model supports DRCLock channel when the Version parameter is set to C_S0024; otherwise, DRCLock channel is not supported and only RPC channel bits are transmitted.

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

1xEV_RevSrc

Description: Reverse link signal generator
Library: 1xEV, Signal Sources
Class: SDF1xEV_RevSrc

Parameters

Name	Description	Default	Unit	Type	Range
DataGain	gain of traffic channel	1		real	(0, ∞)
DRCGain	gain of DRC channel	1		real	(0, ∞)
ACKGain	gain of ACK channel	1		real	(0, ∞)

Pin Inputs

Pin	Name	Description	Signal Type
1	Input	input signal	int

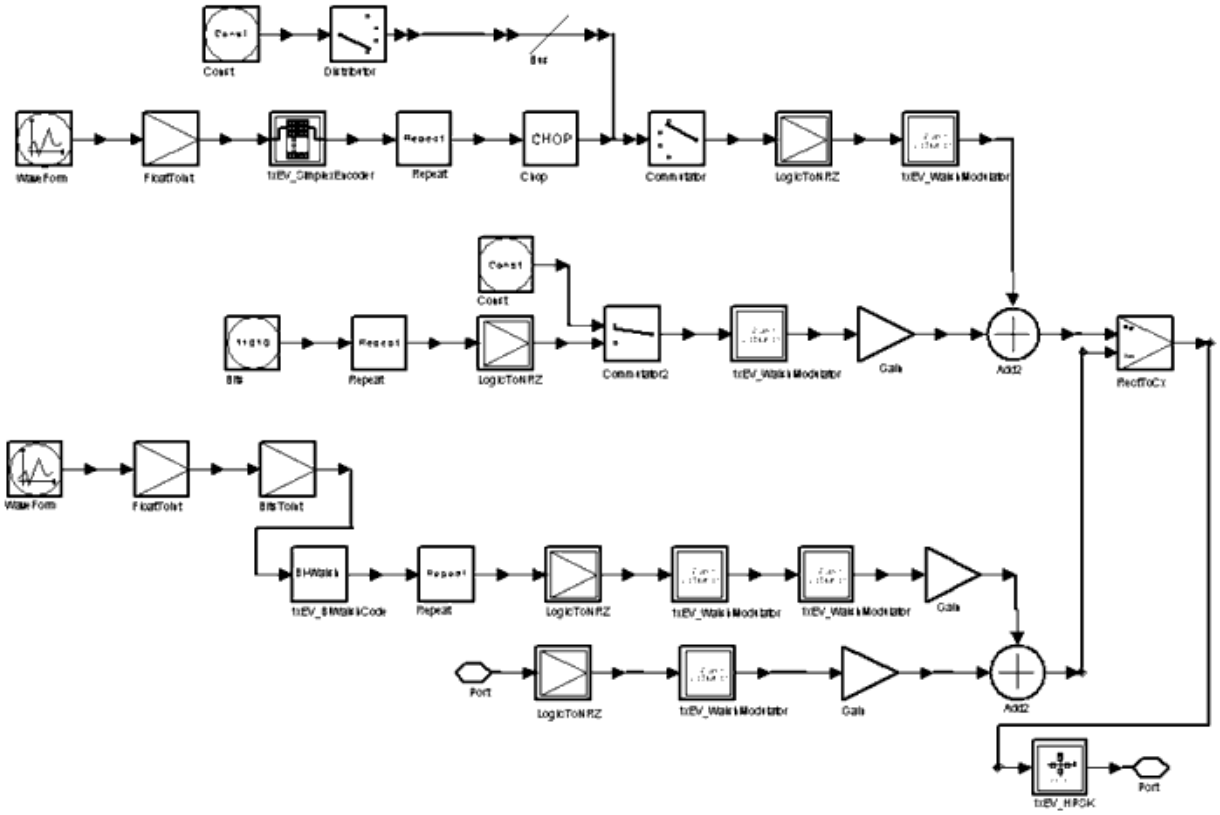
Pin Outputs

Pin	Name	Description	Signal Type
2	Output	output signal	complex

Notes/Equations

1. This subnetwork is used to generate reverse link source signal. The reverse traffic channel consists of a Pilot channel, a reverse rate indicator (RRI) channel, a data rate control (DRC) channel, an acknowledgement (ACK) channel, and a data channel.

   The schematic for this subnetwork is shown in the following figure.



1xEV_RevSrc Schematic

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.

System Bit Error Rate Measurement

Introduction

This workspace validates 1xEV baseband system performance, including BER measurement for both forward and reverse link, in AWGN without channel coding. Designs for these measurements include:

- DSN_1xEV_FwdAWGN_BER for BER performance for forward traffic channel in AWGN without channel coding
- DSN_1xEV_RevAWGN_BER for BER performance for reverse traffic channel in AWGN without channel coding

When RF simulation is performed, noise density is modeled using the AddNDensity component. The defining equation for parameter NDensity is

NDensity(dBm/Hz) = SignalPower(dBm) - 10×log(DataRate) - Eb/N0(dB).

Forward Traffic Channel Bit Error Rate

DSN_1xEV_FwdAWGN_BER

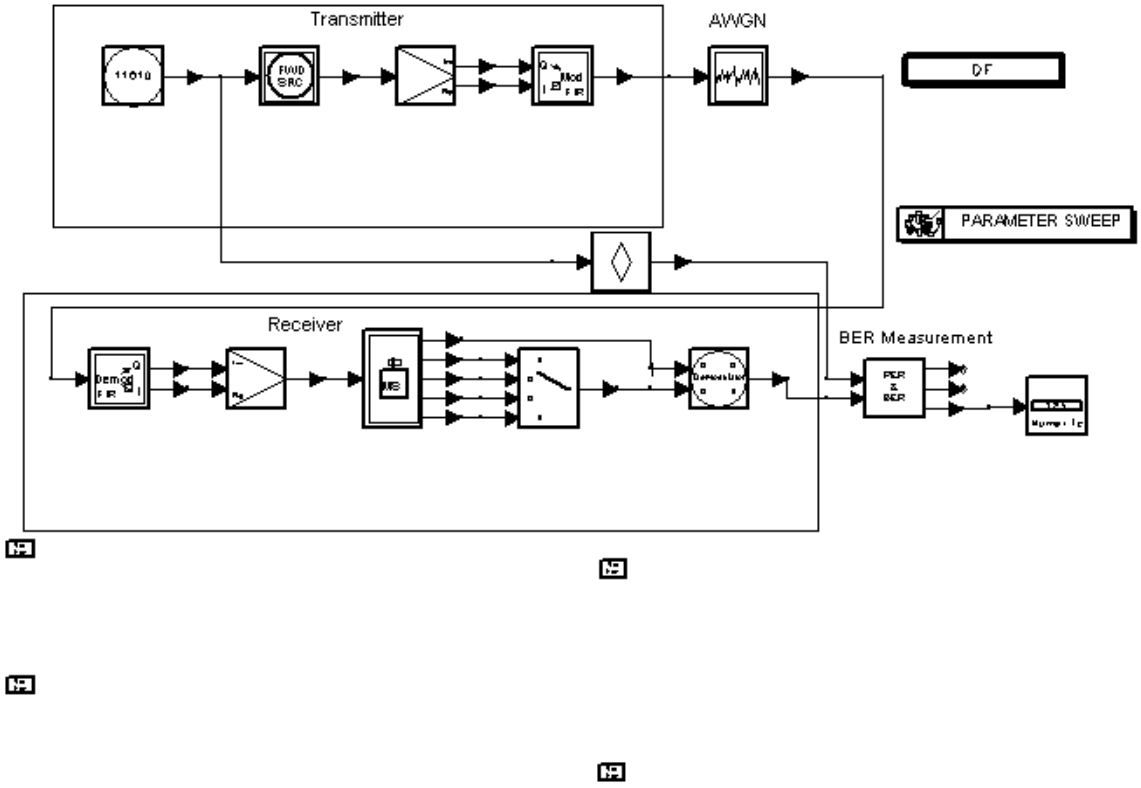
Features

- Curve of BER vs. Eb/N0 of traffic channel is compared with theoretical results.

Description

This example is used to measure BER performance for forward traffic channel in AWGN channel without channel coding. The pilot, MAC, and traffic channels are time division multiplexed. Different data rates can be set using the DataRate parameter.

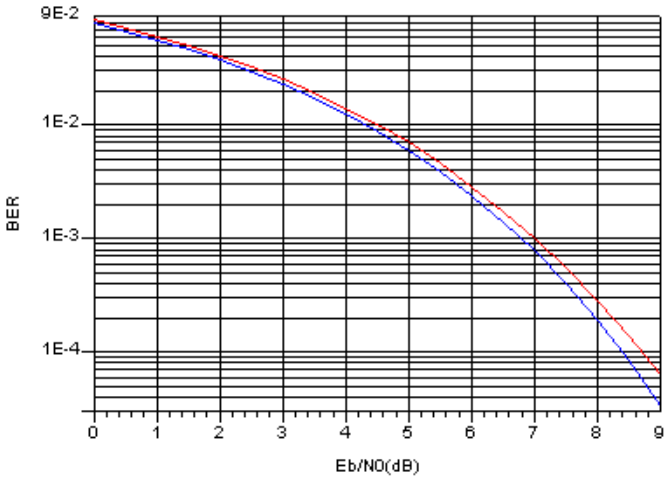
The schematic for this design is shown in the following figure. This design consists of transmitter, AWGN, receiver and BER measurements.



DSN_1xEV_FwdAWGN_BER Schematic

Simulation Results

Test results displayed in DSN_1xEV_FwdAWGN_BER.dds are shown in the following figure.



The blue curve is theoretical results for QPSK under AWGN condition.
The red curve is simulation results for DateRate 0 with QPSK modulation.

Forward Traffic Channel in AWGN without Coding

For forward traffic channel, QPSK, 8PSK and 16QAM are used for different data rates. In the dds file, DataRate is set as 0, i.e., 38.4 kbps is used as an example and QPSK is used. Both theoretical and simulation results are given. For QPSK, the BER is

$$P_b = Q\left(\sqrt{\frac{2E_b}{N_0}}\right)$$

and

$$Q(x) = \frac{1}{\sqrt{2\pi}}\int_x^\infty e^{-t^2/2}dt \qquad (x \geq 0)$$

The curves match well. The performance difference between theoretical and simulation results is caused by calculation and simulation errors.

Benchmark

- Hardware Platform: Pentium II 400 MHz, 512 MB memory
- Software Platform: Windows NT Workstation 4.0, ADS 1.5
- Data Points: 19 points
- Simulation Time: approximately 13.3 hours

References

1. J. G. Proakis, *Digital Communications* , Third Edition.

Reverse Traffic Channel Bit Error Rate

DSN_1xEV_RevAWGN_BER

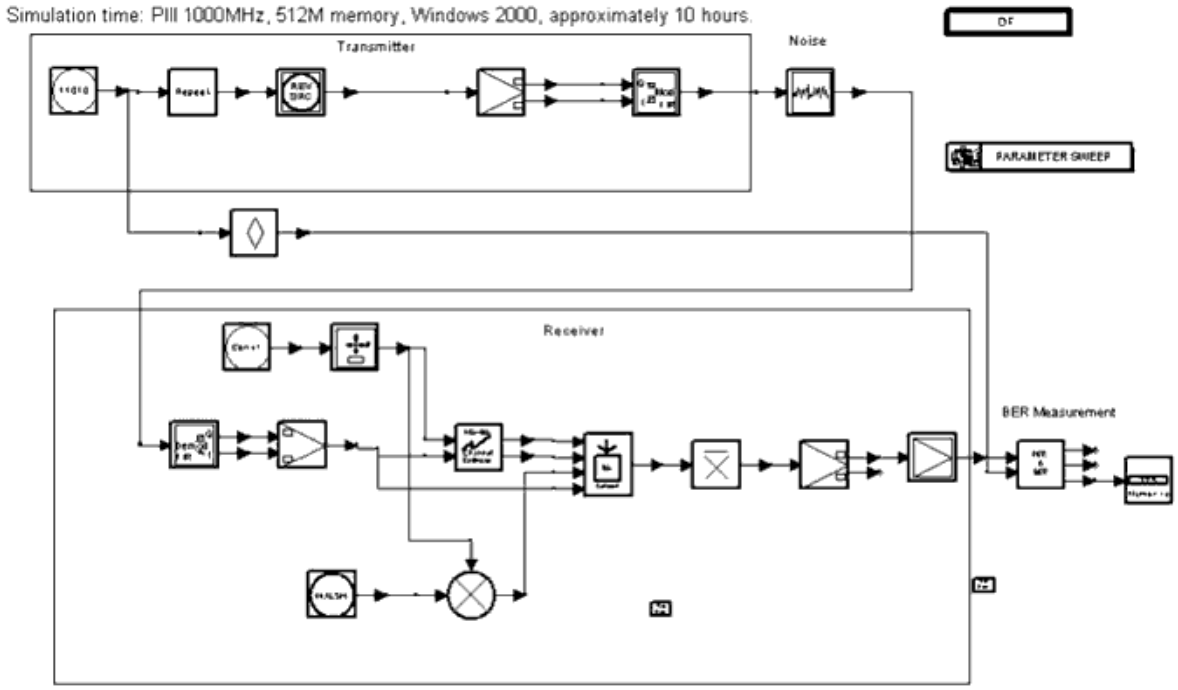
Features

- Curve of BER vs. Eb/N0 of traffic channel is obtained and compared with theoretical results.

Description

This example is used to measure BER performance for reverse traffic channel in AWGN channel without channel coding. One pilot channel and one traffic channel are included. It is assumed that the ratio of signal levels of each channel is 1. The data rate is 38.4 kbps in this example.

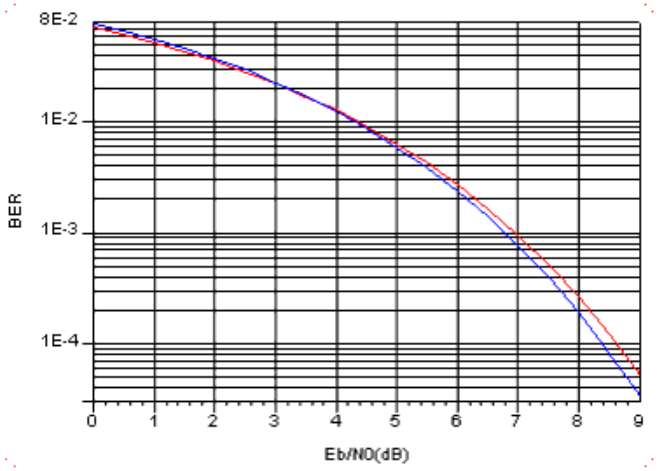
The schematic for this design is shown in the following figure. This design consists of transmitter, AWGN, receiver and BER measurement.



DSN_1xEV_RevAWGN_BER Schematic

Simulation Results

Test results displayed in DSN_1xEV_RevAWGN_BER.dds are shown in the following figure.



The blue curve is theoretical results for QPSK under AWGN condition.
The red curve is simulation results.

Reverse Traffic Channel in AWGN without Coding

For reverse traffic channel, QPSK is used. For QPSK, the BER is

$$P_b = Q\left(\sqrt{\frac{2E_b}{N_0}}\right)$$

and

$$Q(x) = \frac{1}{\sqrt{2\pi}}\int_x^\infty e^{-t^2/2}dt \qquad (x \geq 0)$$

The curves match well. The performance difference between theoretical and simulation results is caused by calculation error and simulation error.

Benchmark

- Hardware Platform: Pentium III 1000 MHz, 512 MB memory
- Software Platform: Windows 2000, ADS 2001
- Data Points: 19 points
- Simulation Time: approximately 10 hours

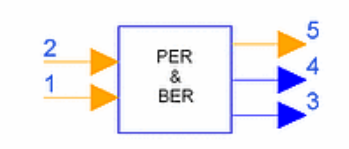
References

1. J. G. Proakis, *Digital Communications* , Third Edition.

Test Components for 1xEV Design Library

- *1xEV BER* (1xev)
- *1xEV FwdCDP* (1xev)
- *1xEV FwdRhoWithRef* (1xev)
- *1xEV PwrMeasure* (1xev)
- *1xEV RevCDP* (1xev)
- *1xEV RevRhoWithRef* (1xev)

1xEV_BER



Description: BER and PER measurement
Library: 1xEV, Test
Class: SDF1xEV_BER

Parameters

Name	Description	Default	Symbol	Unit	Type	Range
Link	type of link: Forward link, Reverse link	Reverse link			enum	
DataRate	data rate of the forward traffic channel, valid when Link=Forward link.: R38.4kbps 16 slot, R76.8kbps 8 slot, R153.6kbps 4 slot, R307.2kbps 2 slot, R614.4kbps 1 slot, R307.2kbps 4 slot, R614.4kbps 2 slot, R1228.8kbps 1 slot, R921.6kbps 2 slot, R1843.2kbps 1 slot, R1228.8kbps 2 slot, R2457.6kbps 1 slot	R38.4kbps 16 slot	R		enum	†
SlotState	state of each slot: 0 for idle, 1 for active, valid when Link=Forward link	1 0 0 0			int array	{0,1}†
PacketLength	packet length	1002	L		int	[1:4074]
IgnoreNumber	number of initially ignored firings	0			int	[0:100]

† DataRate and SlotState are valid only when Link = Forward link.

Pin Inputs

Pin	Name	Description	Signal Type
1	input1	input data 1	int
2	input2	input data 2	int

Pin Outputs

Pin	Name	Description	Signal Type
3	BER	bit error rate	real
4	PER	packet error rate	real
5	Packet	number of packets	int

Notes/Equations

1. This model calculates the BER (bit error rate) and PER (packet error rate) using Monte-Carlo method.

   Each firing,
   - if Link =Forward link, one BER token, one FER token and one Packet token are produced when M input1 tokens and M input2 tokens are consumed; refer to the first of the following tables.
   - If Link = Reverse Link, one BER token, one FER token and one Packet token are produced when L input1 tokens and L input2 tokens are consumed, where L is PacketLength. L for reverse link is MAC given in the second of the following tables.

This model can be a general BER/PER model ignoring 1xEV frame structure by setting Link=Reverse link and setting L to the packet length wanted.

If Link=Forward link, the input should be 4-packet interlace. If the SlotState is {1, 0, 1, 0}, for example, then the first packet and the third packet will be used in calculating BER and PER. The second and fourth packets are fed into this model, but no contribution for the value of BER and PER. If IgnoreNumber is not equal to 0, then the 4-packet interlace should be begun after IgnoreNumber packets.

2. This model counts the number of frames, number of frame errors, and bit errors, then calculates PER and BER using the following equations.

$$PER = \frac{\text{Number of Error Packet}}{\text{Total Packet Number}}$$

$$BER = \frac{\text{Number of Error Bits}}{\text{Total Bit Number}} = \frac{\text{Number of Error Bits}}{\text{Total Packet Number} \times L}$$

This model can support different idle/slot structure for forward link by setting SlotState. If SlotState is set to 1 1 1 1, simulation efficiency can be improved four times.

Forward Traffic Channel Physical Layer Packet Values

Date Rate (kbps)		
Values per Physical Layer Packet		
Slots		
MAC Layer Packet and Pad bits (M) **		
38.4	16	1,002
76.8	8	1,002
153.6	4	1,002
307.2	2	1,002
614.4	1	1,002
307.2	4	2,026
614.4	2	2,026
1,228.8	1	2,026
921.6	2	3,050
1,843.2	1	3,050
1,228.8	2	4,074
2,457.6	1	4,074

Reverse Traffic Channel Physical Layer Packet Values

Physical Layer Packet Bits	**MAC Layer Packet Bits (L)**
256	234
512	490
1024	1002
2048	2026
4096	4074

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1,

August 23, 2001.

1xEV_FwdCDP

Description: Code domain power measurement for forward link
Library: 1xEV, Test
Class: SDF1xEV_FwdCDP

Parameters

Name	Description	Default	Symbol	Unit	Type	Range
Type	channel type for code domain power measurement: Data, MAC	Data			enum	
TestLength	number of slots for code domain power measurement	16	N		int	[1:100]
Q_Phase	sign of sine: Sine, Minus Sine	Sine			enum	
CDP_GroupNum	number of output CDP groups	1	CDP_Num		int	[1, ∞)
PhaseEqualizer	whether the phase equalizer is used at the transmitter: Yes, No	No			enum	

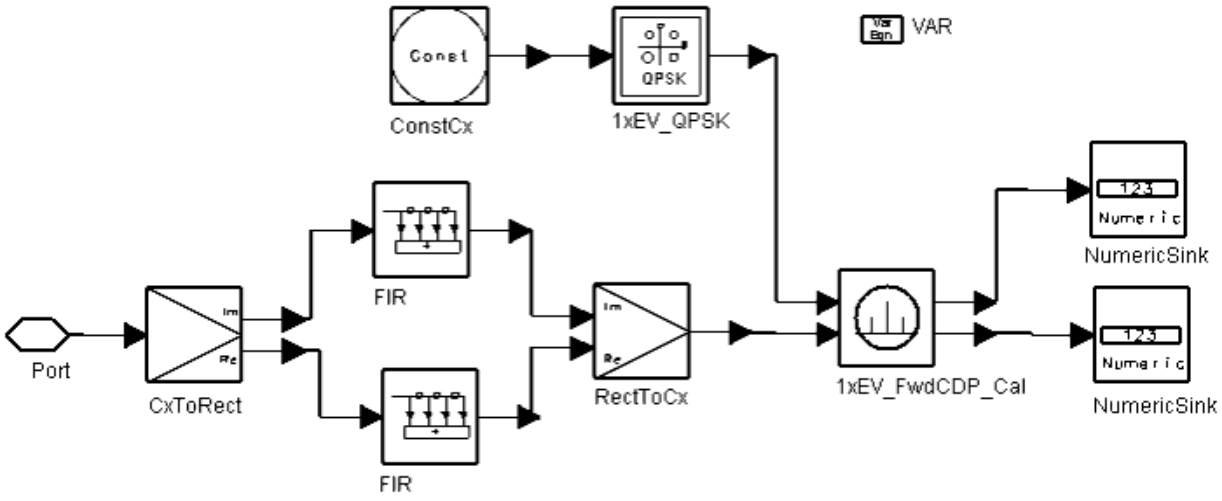
Pin Inputs

Pin	Name	Description	Signal Type
1	SigIn	received base band signal	complex

Notes/Equations

1. This subnetwork is used to measure code domain power for 1xEV reverse link.

   The schematic for this subnetwork is shown in the following figure.



1xEV_FwdCDP Schematic

1xEV_FwdCDP_Cal is the core of the measurement that calculates code domain power. It has two

parameters:

- Type is the channel type for code domain power measurement; it calculates code domain power for the forward traffic and control channel when the value is *Data* and for MAC Channel when the value is *MAC*.
- TestLength is number of slots for code domain power measurement. A frequency offset and a constant initial phase are estimated inside the model for code domain power measurement. It outputs real and imaginary code domain power with two output pins. The sum of real and imaginary powers should add up to 1.0.

  1xEV_FwdCDP_Cal has two input pins: one is the quadrature spreading sequence for the synchronization operations; one is the compensated down-converted input signal. The actual input signal passes through a complementary filter to remove the inter-symbol interference (ISI) introduced by the transmit filter.

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.
2. 3GPP2 C.P9011, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network, Dec.14, 2000.
3. 3GPP2 C.P9012, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Terminal, Dec.14, 2000.

1xEV_FwdRhoWithRef

Description: Rho measurement for forward link
Library: 1xEV, Test
Class: SDF1xEV_FwdRhoWithRef

Parameters

Name	Description	Default	Unit	Type	Range
Type	measurement rho type: pilot, overall-1, overall-2	pilot		enum	
Q_Phase	sign of sine: Sine, Minus Sine	Sine		enum	
EVMValue	EVM value expression options: EVM_Ratio, EVM_Percent	EVM_Ratio		enum	
PhaseEqualizer	whether the phase equalizer is used at the transmitter: Yes, No	No		enum	

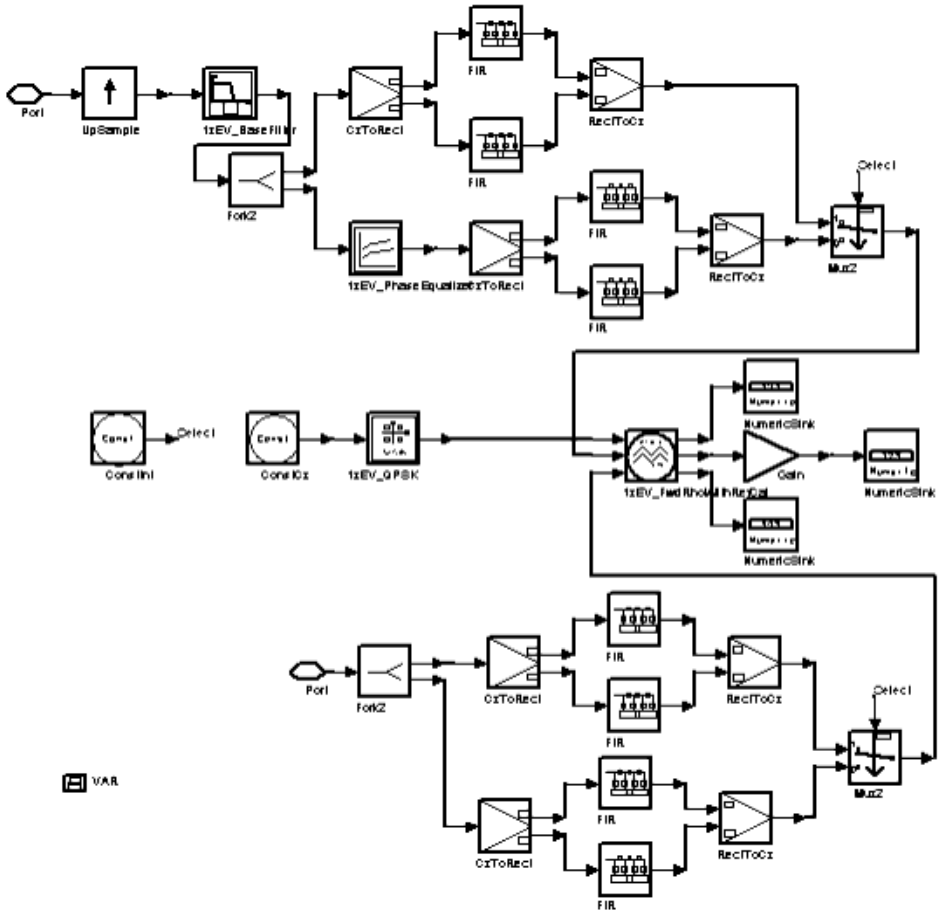
Pin Inputs

Pin	Name	Description	Signal Type
1	SigIn	received base band signal	complex
2	RefIn	reference signals for waveform quality measurement	complex

Notes/Equations

1. This subnetwork measures rho and root mean square error vector magnitude (EVM) for forward link. It estimates frequency error, rho and RMS EVM.

   The schematic for this subnetwork is shown below.



1xEV_FwdRhoWithRef Schematic

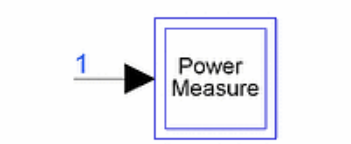
Each firing, 131072 tokens are consumed and one token of Rho, one token of EVM and one token of Dlt_F are collected by three NumericSink components.

2. The EVM and rho are the indexes of modulation accuracy. EVM is obtained by calculating the RMS error vector magnitude between the received signal and the ideal signal. Rho is measured by correlating the received with the reference signal.
3. The actual received signal is passed through a complementary filter to remove the inter-symbol interference (ISI) introduced by the transmit filter.

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.
2. 3GPP2 C.P9011, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network, Dec. 14,2000.
3. 3GPP2 C.P9012, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Terminal, Dec. 14, 2000.

1xEV_PwrMeasure



Description: 1xEV Power measurement
Library: 1xEV, Test
Class: TSDF1xEV_PwrMeasure

Parameters

Name	Description	Default	Unit	Type	Range
SamplesPerSymbol	samples per symbol	4		int	[1:32]
NumHalfSlotsMeasured	number of half slots to be averaged	10		int	[1, ∞)
SignalType	signal type: Baseband signal, RF signal	Baseband signal		enum	
RefR	reference resistance	50.0	Ohm	real	(0, ∞)
RTemp	temperature of resistor	-273.15	Ohm	real	[-273.15, ∞)
IgnoreNum	number of chips to be ignored	1		int	[0, ∞)

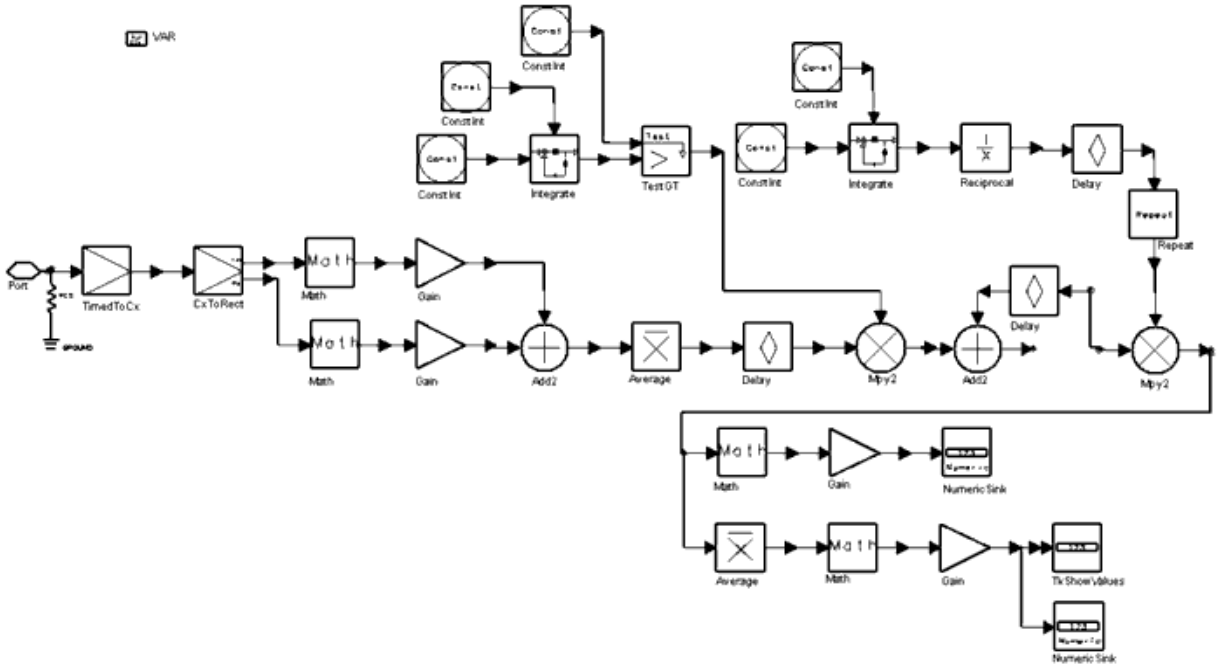
Pin Inputs

Pin	Name	Description	Signal Type
1	SigIn	input signal	timed

Notes/Equation

1. This subnetwork measures the mean transmitted power.

   The schematic for this subnetwork is shown in the following figure.



1xEV_PwrMeasure Schematic

1xEV_RevCDP

Description: Code domain power measurement for reverse link
Library: 1xEV, Test
Class: SDF1xEV_RevCDP

Parameters

Name	Description	Default	Unit	Type	Range
TestLength	number of Walsh periods for measurement	48		int	[1:100]
SampleRate	number of samples per chip	4		int	[1:32]
CDP_GroupNum	number of output CDP groups	1		int	[1, ∞)

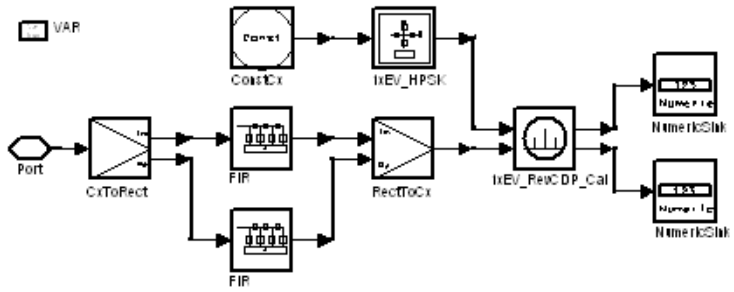
Pin Inputs

Pin	Name	Description	Signal Type
1	SigIn	received baseband signal	complex

Notes/Equations

1. This subnetwork measures code domain power for 1xEV reverse link.

   The schematic for this subnetwork is shown in the following figure.



1xEV_RevCDP Schematic

   1xEV_RevCDP_Cal has two input pins: one is the quadrature spreading sequence for the synchronization operations; one is the compensated down-converted input signal. The actual input signal passes through a complementary filter to remove the inter-symbol interference introduced by the transmit filter. The code power is mapped onto 16 code channels.

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1,

August 23, 2001.
2. 3GPP2 C.P9011, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network, Dec.14, 2000.
3. 3GPP2 C.P9012, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Terminal, Dec.14, 2000.

1xEV_RevRhoWithRef

Description: Rho measurement for reverse link
Library: 1xEV, Test
Class: SDF1xEV_RevRhoWithRef

Parameters

Name	Description	Default	Unit	Type	Range
Q_Phase	sign of sine: Sine, Minus Sine	Sine		enum	
StartSym	start symbol for EVM measurement	256		int	[0:15359]
SymBurstLen	number of symbols within burst to be measured for EVM	1024		int	[1:16384]
EVMValue	EVM value expression options: EVM_Ratio, EVM_Percent	EVM_Ratio		enum	

Pin Inputs

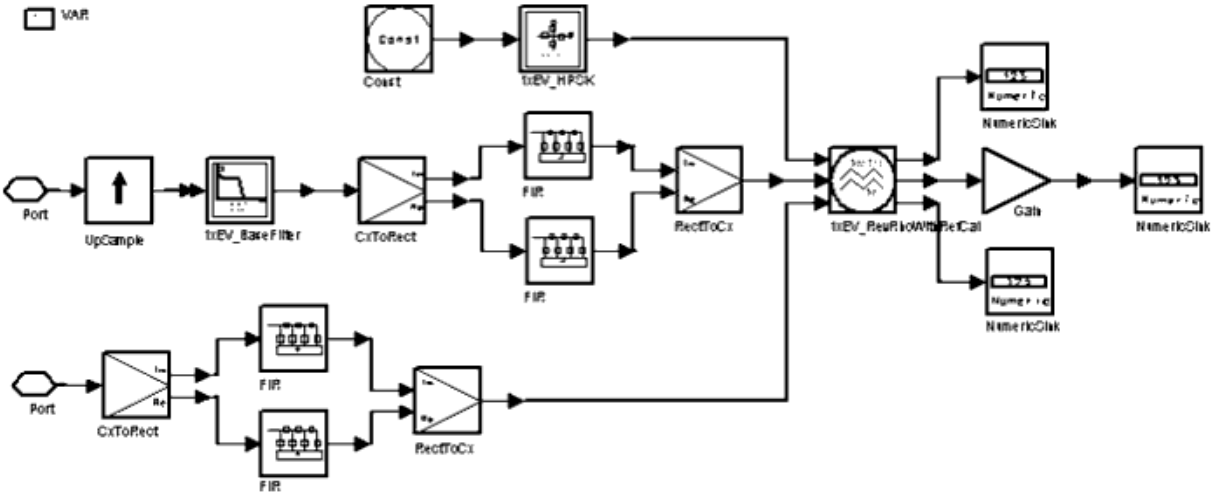
Pin	Name	Description	Signal Type
1	SigIn	received base band signal	complex
2	RefIn	reference signals for waveform quality measurement	complex

Notes/Equations

1. This component is used to measure rho and root mean square error vector magnitude (EVM) for reverse link. It estimates frequency error, rho and RMS EVM.

   The schematic for this subnetwork is shown in the following figure.

   Each firing, 131072 tokens are consumed and one token of Rho, one token of EVM and one token of Dlt_F are collected by three NumericSink components.



1xEV_RevRhoWithRef Schematic

2. The EVM and rho are the indexes of modulation accuracy. EVM is obtained by calculating the RMS error vector magnitude between the received signal and the ideal signal. Rho is measured by correlating the received with the reference signal.
3. The actual received signal is passed through a complementary filter to remove the inter-symbol interference (ISI) introduced by the transmit filter.

References

1. 3GPP2 C.S0024, *cdma2000 High Rate Packet Data Air Interface Specification* , Version 2.1, August 23, 2001.
2. 3GPP2 C.P9011, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Network, Dec. 14, 2000.
3. 3GPP2 C.P9012, Recommended Minimum Performance Standards for cdma2000 High Rate Packet Data Access Terminal, Dec.14, 2000.